Solid State Devices, Inc.
14701 Firestone Blvd * La Mirada, CA 90638
Phone: (562) 404-7855 * Fax: (562) 404-1773
ssdi@ssdi-power.com * www.ssdi-power.com

SFT5094 and SFT5096
Series

1 AMP, 500 Volts
High Voltage PNP Transistor

DESIGNER'S DATA SHEET

Part Number / Ordering Information 1/

SFT5094
SFT5096

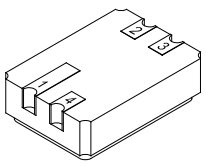
Screening 2/ __ = No Screening
TX = TX Level
TXV = TXV Level
S = S Level

Package 3/ -4 = 4 Pin CLCC
/5 = TO-5
G = CERPACK
S22 = SMD.22

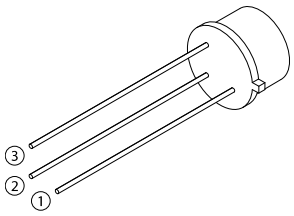
Features:
- BV_{CER} to 500 Volts
- Low Leakage at High Temperature
- High Linear Gain, Low Saturation Voltage
- 200°C Operating Temperature
- Gold Eutectic Die Attach
- TX, TXV, S-Level Screening Available
- Designed for Complementary Use with SFT5015
- Replacement for 2N5094 and 2N5096 with Lower Thermal Resistance
- Available with TO-5, Cerpack, CLCC, and SMD.22 Cases

Maximum Ratings 4/		Symbol	SFT5094	SFT5096	Units
Collector – Emitter Voltage		**V_{CEO}**	350	400	**Volts**
(R_{BE} = 1kΩ)		**V_{CER}**	450	500	**Volts**
Collector – Base Voltage		**V_{CBO}**	450	500	**Volts**
Emitter – Base Voltage		**V_{EBO}**	6		**Volts**
Collector Current		**I_C**	1.0		**Amps**
Base Current		**I_B**	0.5		**Amps**
Total Power Dissipation	(T_C = 25ºC)	**P_D**	1.0		**Watts**
	(T_A = 25ºC)		0.4		**Watts**
Derate above T_C = 25ºC			5.7		**mW /ºC**
Operating & Storage Temperature		**T_J & T_{STG}**	-65 to +200		**ºC**
Maximum Thermal Resistance	4 Pin CLCC	**$R_{\theta JC}$**	175		**ºC/W**
(Junction to Case)	TO-5		30		**ºC/W**
	CERPACK		9		**ºC/W**
	SMD.22		9		
Maximum Thermal Resistance	4 Pin CLCC	**$R_{\theta JA}$**	440		**ºC/W**
(Junction to Ambient)	TO-5		---		**ºC/W**
	CERPACK		440		**ºC/W**
	SMD.22		440		

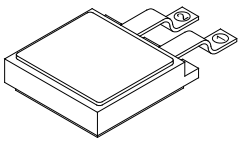
4 Pin CLCC (-4)



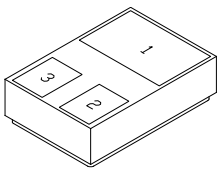
TO-5 (/5)



CERPACK (G)



SMD.22 (S22)



NOTES:
1/ For Ordering Information, Price, Operating Curves, and Availability Contact Factory.
2/ Screened to MIL-PRF-19500.
3/ For Package Outlines, See Figure 1.
4/ Unless Otherwise Specified, Maximum Ratings/Electrical Characteristics at 25°C.

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Electrical Characteristics [4/]		Symbol	Min		Max	Units
			SFT5094	SFT5096		
Collector – Emitter Breakdown Voltage *	(I_C = 5 mA)	BV_{CEO}	350	400	—	Volts
	(I_C = 100 µA, R_{BE} = 1k Ω)	BV_{CER}	450	500	—	
Collector – Base Breakdown Voltage *	(I_C = 100 µA)	BV_{CBO}	450	500	—	Volts
Emitter – Base Breakdown Voltage	(I_E = 50 µA)	BV_{EBO}	6		—	Volts
Collector Cutoff Current	(V_{CB} = Rated, T_A = 25°C)	I_{CBO1}	—		1.0	µA
	(V_{CB} = Rated, T_A = 100°C)	I_{CBO2}	—		50	
Emitter Cutoff Current	(V_{EB} = 6 V)	I_{EBO}	—		1.0	µA
DC Current Gain *	(I_C = 1 mA, V_{CE} = 10 V)	H_{FE}	20		250	
	(I_C = 25 mA, V_{CE} = 10 V)		40		300	
	(I_C = 100 mA, V_{CE} = 10 V)		20		250	
Collector-Emitter Saturation Voltage *	(I_C = 25 mA, I_B = 2.5 mA)	$V_{CE\ (SAT)}$	—		500	mV
Base-Emitter Saturation Voltage	(I_C = 25 mA, I_B = 2.5 mA)	$V_{BE\ (SAT)}$	—		1.0	Volts
Current Gain Bandwidth Product *	(I_C = 10 mA, V_{CE} = 10 V, f = 10 MHz)	f_T	25		—	MHz
Output Capacitance	V_{CB} = 20 V, I_E = 0 A, f = 1.0MHz	C_{ob}	—		10	pF
Turn on Delay Time	V_{CC}= 100 V	T_d	—		500	ns
Rise Time	I_C= 100 mA	T_r	—		1200	ns
Storage Time	I_{B1} = I_{B2} = 10 mA	T_s	—		2.0	µs
Fall Time		t_f	—		500	ns

Notes: * Pulse Test: Pulse Width = 300 µs. Duty Cycle = 2%.

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PIN ASSIGNMENT (Standard)			
Package	**Collector**	**Emitter**	**Base**
4 Pin CLCC (-4)	Pin 1	Pin 2	Pin 3
TO-5 (/5)	Pin 3	Pin 1	Pin 2
CERPACK (G)	CASE	Pin 1	Pin 2
SMD.22	Pin 1	Pin 2	Pin 3

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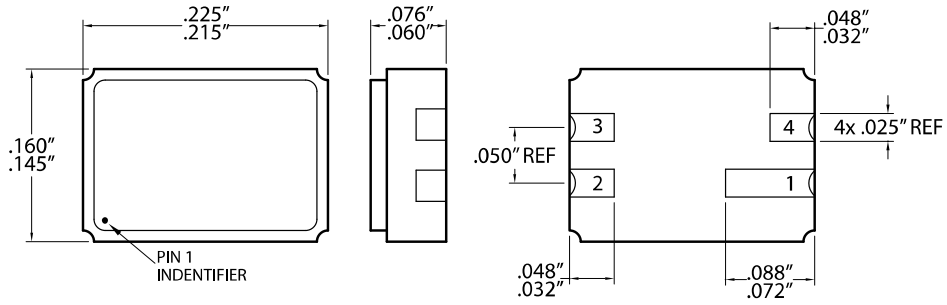
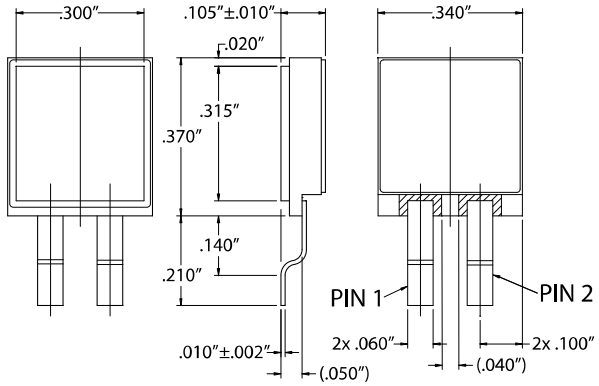
FIGURE 1 – CASE OUTLINES

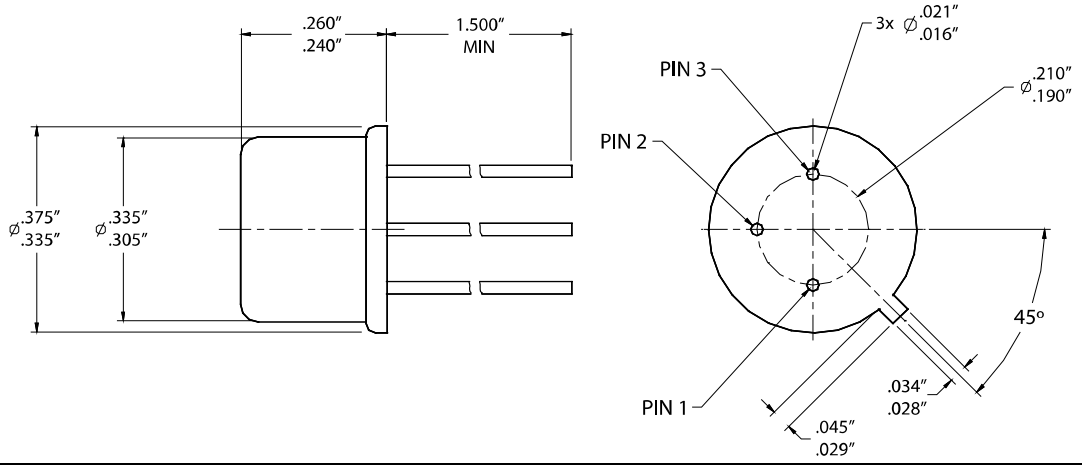
4 Pin CLCC (-4):



CERPACK (G):



TO-5 (/5):



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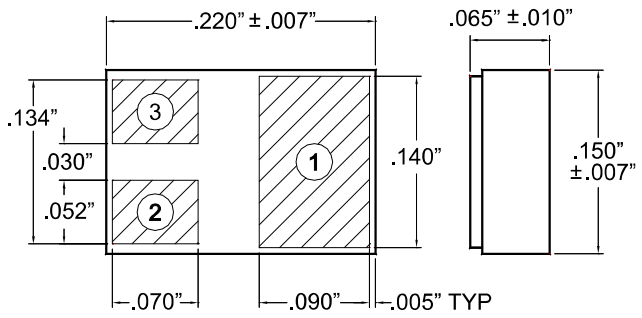

NOTE: All specifications are subject to change without notification. SCD's for these devices should be reviewed by SSDI prior to release.	DATA SHEET #: TR0081E	DOC