Solid State Devices, Inc.
14701 Firestone Blvd * La Mirada, CA 90638
Phone: (562) 404-4474 * Fax: (562) 404-1773
ssdi@ssdi-power.com * www.ssdi-power.com

SFF130G
SFF130S.5

DESIGNER'S DATA SHEET

14 AMP, 100 Volts, 180 mΩ Avalanche Rated N-channel Power MOSFET

Part Number / Ordering Information 1/

SFF130 __ __

__ **Screening** 2/
- __ = Not Screened
- TX = TX Level
- TXV = TXV Level
- S = S Level

Package
- G = Cerpack
- S.5 = SMD.5

Features:
- Rugged Technology
- Low ON-Resistance: 130mΩ typ
- Avalanche Rated
- Hermetically Sealed Power Packaging
- Low Total Gate Charge, Fast Switching
- Enhanced Performance Replacement for 2N6756
- TX, TXV, S-Level Screening Available

Maximum Ratings 3/		Symbol	Value	Unit
Drain – Source Voltage		V_{DSS}	100	V
Gate – Source Voltage, continuous **Gate – Source Voltage, transient**		V_{GS}	±20 ±30	V
Max. Continuous Drain Current (package limited)	**@ T_C = 25°C** **@ T_C = 100°C**	I_{D1} I_{D2}	14 9	A
Max. Avalanche Current		I_{AR}	14	A
Single Pulse Avalanche Energy		E_{AS}	75	mJ
Repetitive Pulse Avalanche Energy		E_{AR}	7.5	mJ
Total Power Dissipation @ T_C = 25°C	**@ T_C = 25°C** **@ T_C = 55°C**	P_D	44 34	W
Operating & Storage Temperature		T_{OP} & T_{STG}	-55 to +150	°C
Maximum Thermal Resistance (Junction to Case)		$R_{\theta JC}$	2.8	°C/W

NOTES:
1/ For ordering information, price, and availability - contact factory.
2/ Screening based on MIL-PRF-19500. Screening flows available on request.
3/ Unless otherwise specified, all electrical characteristics @ 25°C.

SMD.5 (S.5) **Cerpack (G)**

NOTE: All specifications are subject to change without notification. SCD's for these devices should be reviewed by SSDI prior to release.	DATA SHEET #: F00021E	DOCX

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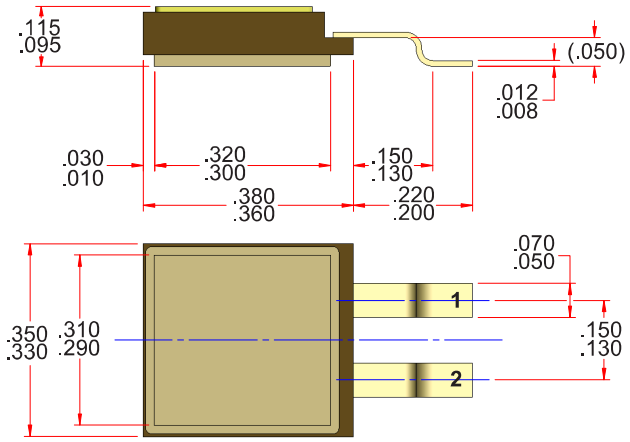
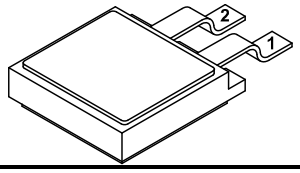
Electrical Characteristics [3/]		Symbol	Min	Typ	Max	Unit
Drain to Source Breakdown Voltage	V_{GS} = 0 V, I_D =0.25 mA	BV_{DSS}	100	115	-	V
Drain to Source On State Resistance	V_{GS} = 10 V, I_D = 9 A V_{GS} = 10 V, I_D = 14 A	$R_{DS(on)}$	- --	125 130	180 210	mΩ
Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 0.25 mA	$V_{GS(th)}$	2.0	2.8	4.0	V
Gate to Source Leakage	V_{GS} = ±20 V	I_{GSS}	-	1	±100	nA
Zero Gate Voltage Drain Current	V_{DS} = 80 V, V_{GS} = 0 V, T_J = 25°C V_{DS} = 80 V, V_{GS} = 0 V, T_J = 125°C	I_{DSS}	- -	0.01 1	25 250	µA µA
Forward Transconductance	V_{DS} = 10 V, I_D = 9 A	g_{fs}	4.6	7	-	Mho
Total Gate Charge **Gate to Source Charge** **Gate to Drain Charge**	V_{GS} = 10 V V_{DS} = 50 V I_D = 14 A	Q_g Q_{gs} Q_{gd}	12 2.5 5	16 4 6.5	35 10 15	nC
Turn on Delay Time **Rise Time** **Turn off Delay Time** **Fall Time**	V_{GS} = 10 V V_{DS} = 50 V I_D = 14 A R_G = 7.5 Ω	$t_{d(on)}$ t_r $t_{d(off)}$ t_f	- - - -	18 70 35 10	35 80 60 45	nsec
Diode Forward Voltage	I_F = 14 A, V_{GS} = 0 V	V_{SD}	-	1.15	1.5	V
Diode Reverse Recovery Time **Reverse Recovery Charge**	I_F = 10 A, di/dt = 100 A/µsec	t_{rr} Q_{rr}	- -	140 1	300 3	nsec µC
Input Capacitance **Output Capacitance** **Reverse Transfer Capacitance**	V_{GS} = 0 V V_{DS} = 25 V f = 1 MHz	C_{iss} C_{oss} C_{rss}	- - -	650 250 44	- - -	pF

PACKAGE OUTLINE: Cerpack (G)

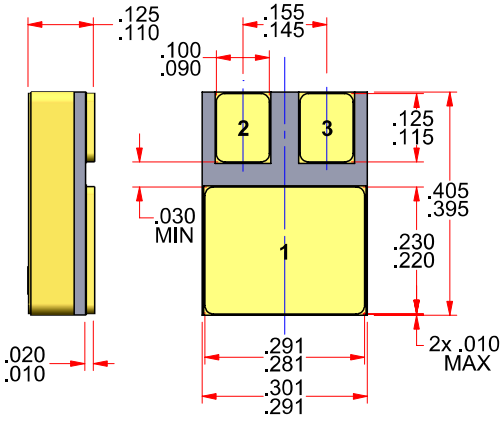


Bottom View

PINOUT:
PIN 1: SOURCE
PIN 2: GATE
BOTTOM PAD: DRAIN

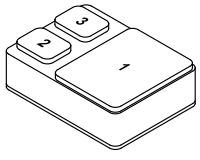


PACKAGE OUTLINE: SMD.5 (S.5)



Bottom View

PINOUT:
PIN 1: DRAIN
PIN 2: SOURCE
PIN 3: GATE



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