



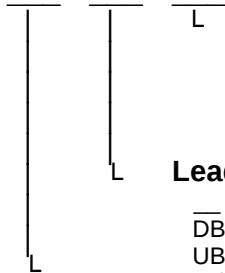
Solid State Devices, Inc.

14701 Firestone Blvd * La Mirada, Ca 90638
Phone: (562) 404-4474 * Fax: (562) 404-1773
ssdi@ssdi-power.com * www.ssdi-power.com

DESIGNER'S DATA SHEET

Part Number / Ordering Information ^{1/}

SFF80N20



Screening ^{2/}

— = Not Screened
TX = TX Level
TXV = TXV Level
S = S Level

Lead Option

— = Straight Leads
DB = Down Bend
UB = Up Bend

Package ^{3/}

J = TO-257 Z = TO-254Z
M = TO-254 N = TO-258

SFF80N20 Series

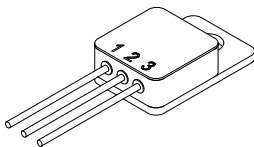
80 AMP , 200 Volts, 15 mΩ Avalanche Rated N-channel MOSFET

Features:

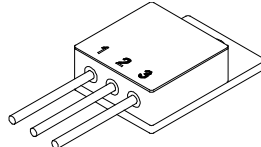
- Rugged poly-Si gate
- Lowest ON-resistance in the industry
- Avalanche rated
- Hermetically Sealed, Isolated Package
- Low Total Gate Charge
- Fast Switching
- TX, TXV, S-Level screening available
- Improved ($R_{DS(ON)}$) Q_G figure of merit

Maximum Ratings ^{4/}		Symbol	Value	Unit
Drain - Source Voltage		V_{DSS}	200	V
Gate - Source Voltage	continuous transient	V_{GS}	± 20 ± 30	V
Max. Continuous Drain Current (package limited)	@ $T_C = 25^\circ C$	I_{D1}	55	A
Max. Instantaneous Drain Current (T_j limited)	@ $T_C = 25^\circ C$ @ $T_C = 175^\circ C$	I_{D2} I_{D3}	80 48	A
Max. Avalanche Current	@ $L = 0.1$ mH	I_{AR}	80	A
Single and Repetitive Avalanche Energy	@ $I_D = 80$ A	E_{AS}	500	mJ
Total Power Dissipation	@ $T_C = 25^\circ C$	P_D	150	W
Operating & Storage Temperature		T_{OP} & T_{STG}	-55 to +175	$^\circ C$
Maximum Thermal Resistance (Junction to Case)		$R_{\theta JC}$	0.55 (typ.0.4)	$^\circ C/W$

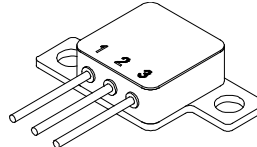
TO-257 (J)



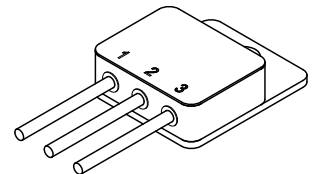
TO-254 (M)



TO-254Z (Z)



TO-258 (N)



NOTES:

*Pulse Test: Pulse Width = 300 μ sec, Duty Cycle = 2%.

^{1/} For ordering information, price, and availability - contact factory.

^{2/} Screening based on MIL-PRF-19500. Screening flows available on request.

^{3/} Maximum current limited by package configuration.

^{4/} Unless otherwise specified, all electrical characteristics @25 $^\circ C$.

NOTE: All specifications are subject to change without notification.
SCD's for these devices should be reviewed by SSDI prior to release.

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SFF80N20 Series

Electrical Characteristics ^{4/}		Symbol	Min	Typ	Max	Unit
Drain to Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 1 \text{ mA}$	BV_{DSS}	200	215	—	V
Drain to Source On State Resistance	$V_{GS} = 10 \text{ V}, I_D = 80 \text{ A}, T_j = 25^\circ\text{C}$	$R_{DS(on)}$	—	15	20	mΩ
	$V_{GS} = 10 \text{ V}, I_D = 80 \text{ A}, T_j = 125^\circ\text{C}$		—	25	35	
	$V_{GS} = 10 \text{ V}, I_D = 80 \text{ A}, T_j = 175^\circ\text{C}$		—	35	—	
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = .25 \text{ mA}, T_j = 25^\circ\text{C}$	$V_{GS(th)}$	2.0	3.0	4.0	V
	$V_{DS} = V_{GS}, I_D = .25 \text{ mA}, T_j = 125^\circ\text{C}$		1.0	2.1	—	
	$V_{DS} = V_{GS}, I_D = .25 \text{ mA}, T_j = -55^\circ\text{C}$		—	3.5	5	
Gate to Source Leakage	$V_{GS} = \pm 20 \text{ V}, T_j = 25^\circ\text{C}$	I_{GSS}	—	10	±100	nA
	$V_{GS} = \pm 20 \text{ V}, T_j = 125^\circ\text{C}$		—	30	—	
Zero Gate Voltage Drain Current	$V_{DS} = 200 \text{ V}, V_{GS} = 0 \text{ V}, T_j = 25^\circ\text{C}$	I_{DSS}	—	0.1	1	μA
	$V_{DS} = 200 \text{ V}, V_{GS} = 0 \text{ V}, T_j = 125^\circ\text{C}$		—	10	100	μA
	$V_{DS} = 200 \text{ V}, V_{GS} = 0 \text{ V}, T_j = 175^\circ\text{C}$		—	250	—	μA
Forward Transconductance	$V_{DS} = 2.50 \text{ V}, I_D = 80 \text{ A}, T_j = 25^\circ\text{C}$	g_{fs}	50	70	—	Mho
Total Gate Charge	$V_{GS} = 10 \text{ V}$	Q_g	—	65	100	nC
Gate to Source Charge	$V_{DS} = 100 \text{ V}$	Q_{gs}	—	24	35	
Gate to Drain Charge	$I_D = 44 \text{ A}$	Q_{gd}	—	13	20	
Turn on Delay Time	$V_{GS} = 10 \text{ V}$	$t_{d(on)}$	—	35	75	nsec
Rise Time	$V_{DS} = 100 \text{ V}$	t_r	—	32	65	
Turn off Delay Time	$I_D = 44 \text{ A}$	$t_{d(off)}$	—	65	125	
Fall Time	$R_G = 1.6 \Omega, pw = 3 \mu\text{s}$	t_f	—	20	45	
Diode Forward Voltage	$I_F = 88 \text{ A}, V_{GS} = 0 \text{ V}$	V_{SD}	—	1.35	1.5	V
Diode Reverse Recovery Time	$I_F = 44 \text{ A}, di/dt = 100 \text{ A}/\mu\text{sec}$	t_{rr}	—	160	200	nsec
Reverse Recovery Charge		Q_{rr}	—	850	—	nC
Input Capacitance	$V_{GS} = 0 \text{ V}$	C_{iss}	—	6200	—	pF
Output Capacitance	$V_{DS} = 100 \text{ V}$	C_{oss}	—	400	—	
Reverse Transfer Capacitance	$f = 1 \text{ MHz}$	C_{rss}	—	—	—	

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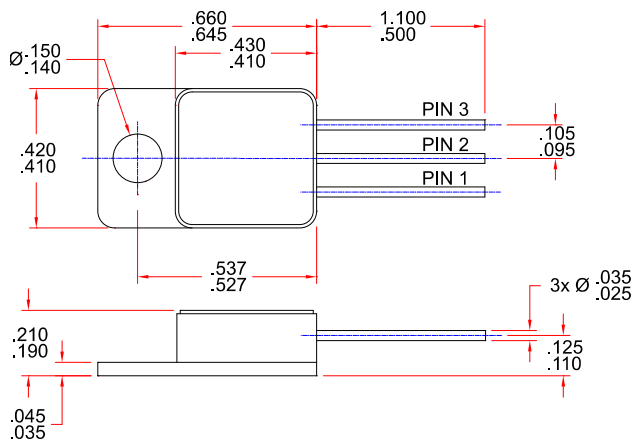
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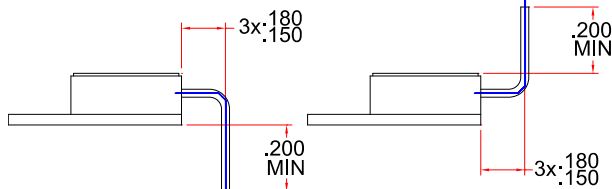
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SFF80N20 Series

TO-257 (J)



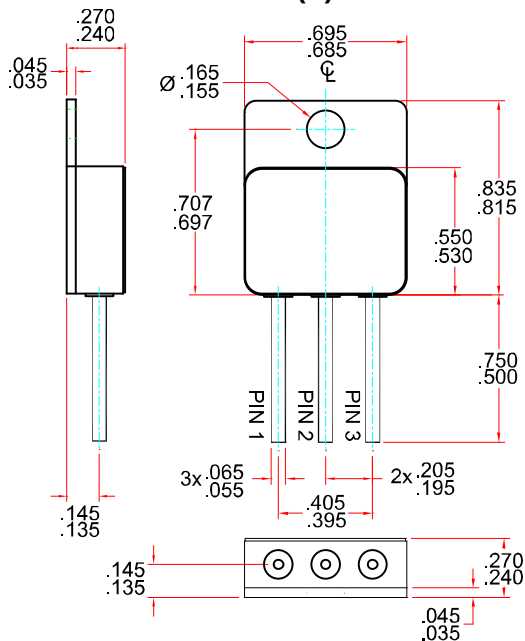
Lead Bend Options: TO-257 (J)



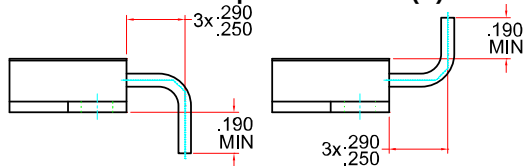
Down Bend (JDB)

Up Bend (JUB)

TO-258 (N)



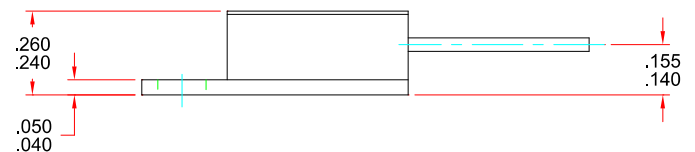
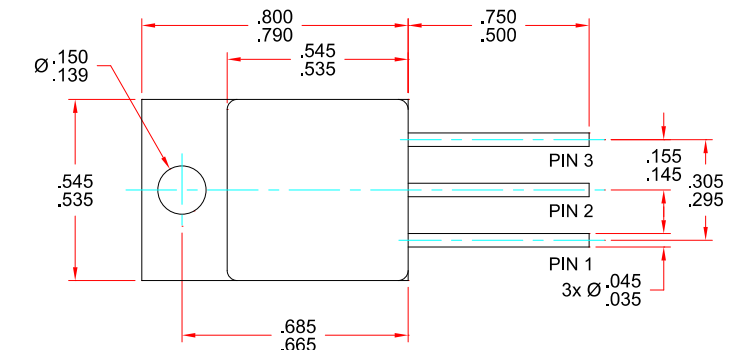
Lead Bend Options: TO-258 (N)



Down Bend (NDB)

Up Bend (NUB)

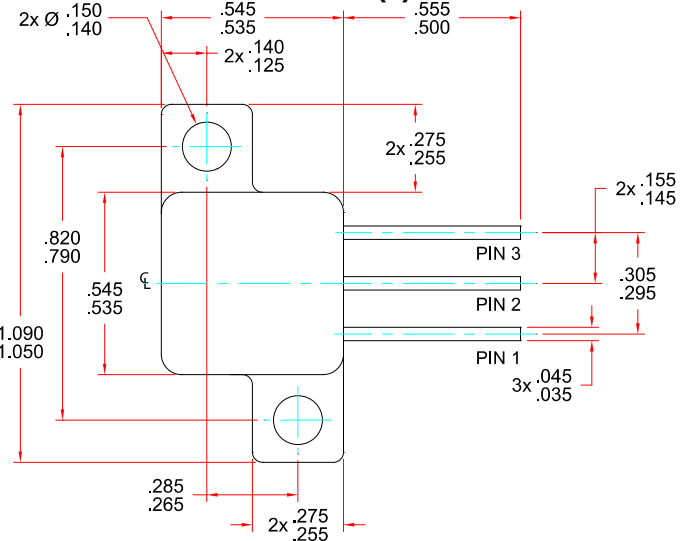
TO-254 (M)



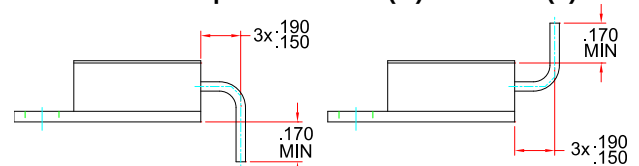
Down Bend (MDB / ZDB)

Up Bend (MUB / ZUB)

TO-254Z (Z)



Lead Bend Options: TO-254 (M) / TO-254Z (Z)



PIN ASSIGNMENT (Standard)

Package	Drain	Source	Gate
TO-257, TO-254, TO-254Z, TO-258	Pin 1	Pin 2	Pin 3

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