Solid State Devices, Inc.
14701 Firestone Blvd * La Mirada, Ca 90638
Phone: (562) 404-4474 * Fax: (562) 404-1773
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SFF13N100/3

13 AMP, 1000 Volts, 340 mΩ Avalanche Rated N-Channel MOSFET

DESIGNER'S DATA SHEET

Part Number / Ordering Information [1/]

SFF13N100

Screening [2/]
- __ = Not Screened
- TX = TX Level
- TXV = TXV Level
- S = S Level

Package
- /3 = TO-3

Features:
- Rugged Poly-Si Gate
- Lowest ON-Resistance in the Industry
- Avalanche Rated
- Hermetically Sealed Power Package
- Ceramic Seals for Improved Hermeticity
- Low Total Gate Charge
- Fast Switching
- Fast Recovery and Superior dv/dt Performance
- Low Input and Transfer Capacitance for Easy Paralleling
- TX, TXV, S-Level Screening Available
- Improved ($R_{DS(ON)}$ Q_G) Figure of Merit
- Replacement for IXTH10N100 Types

Maximum Ratings [3/]		Symbol	Value	Unit
Drain – Source Voltage		V_{DSS}	1000	V
Gate – Source Voltage	continuous transient	V_{GS}	±20 ±30	V
Continuous Drain Current (T_{OP} limited) @ T_C = 25°C		I_{D1}	13	A
Continuous Drain Current (T_{OP} limited) @ T_C = 100°C		I_{D2}	8	A
Pulsed Drain Current (P_{width} /T_{OP} limited) @ T_C = 25°C		I_{D3}	40	A
Single and Repetitive Avalanche Energy		E_{AS} E_{AR}	650 1	mJ
Total Power Dissipation @ T_C = 25°C		P_D	150	W
Operating & Storage Temperature		T_{OP} & T_{STG}	-55 to +150	°C
Maximum Thermal Resistance (Junction to Case)		$R_{\theta JC}$	0.83	°C/W

NOTES: *Pulse Test: Pulse Width = 300μsec, Duty Cycle = 2%.
1/ For ordering information, price, and availability - contact factory.
2/ Screening based on MIL-PRF-19500. Screening flows available on request.
3/ Unless otherwise specified, all electrical characteristics @25°C.

TO-3 (/3)

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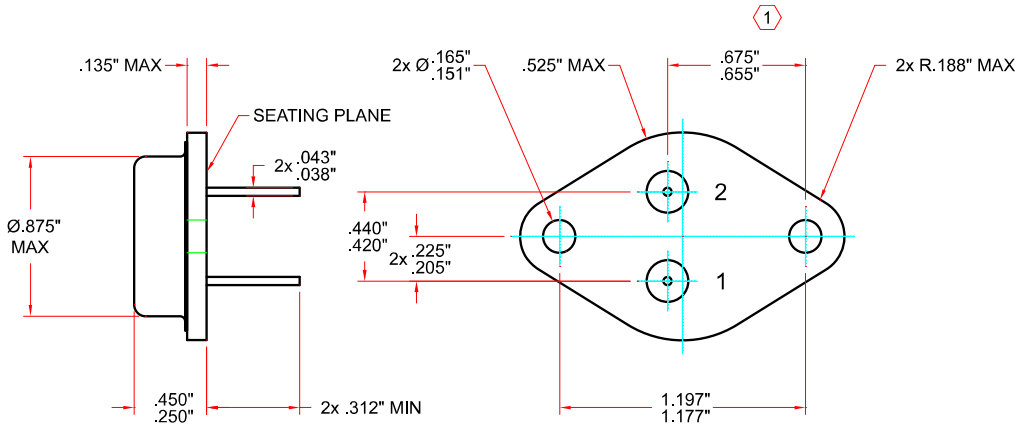
Electrical Characteristics[5/]		Symbol	Min	Typ	Max	Unit
Drain to Source Breakdown Voltage	V_{GS} = 0 V, I_D = 0.25 mA	BV_{DSS}	1000	1030	—	V
Drain to Source On State Resistance	V_{GS} = 10 V, I_D = 10 A, Tj = 25°C V_{GS} = 10 V, I_D = 10 A, Tj = 150°C	$R_{DS(on)}$	— —	310 830	340 —	mΩ
Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 1 mA, Tj = 25°C V_{DS} = V_{GS}, I_D = 1 mA, Tj = 125°C V_{DS} = V_{GS}, I_D = 1 mA, Tj = -55°C	$V_{GS(th)}$	2.5 1.5 —	3.0 2.0 4.0	3.5 — 4.5	V
Gate to Source Leakage	V_{GS} = ±20 V, Tj = 25°C V_{GS} = ±20 V, Tj = 125°C	I_{GSS}	— —	1 10	±100 —	nA
Zero Gate Voltage Drain Current	V_{DS} = 900 V, V_{GS} = 0 V, T_j = 25°C V_{DS} = 900 V, V_{GS} = 0 V, T_j = 150°C	I_{DSS}	— —	0.01 6	2 150	µA µA
Total Gate Charge Gate to Source Charge Gate to Drain Charge	V_{GS} = 10 V V_{DS} = 150 V I_D = 10 A	Q_g Q_{gs} Q_{gd}	— — —	95 12 38	150 25 60	nC
Turn on Delay Time Rise Time Turn off Delay Time Fall Time	V_{GS} = 10 V V_{DS} = 150 V I_D = 10 A	$t_{d(on)}$ t_r $t_{d(off)}$ t_f	— — — —	35 17 130 13	75 25 200 40	nsec
Diode Forward Voltage	I_F = 10 A, V_{GS} = 0 V	V_{SD}	—	0.88	1.1	V
Diode Reverse Recovery Time Reverse Recovery Charge	I_F = 10 A, di/dt = 100 A/µsec I_F = 10 A, di/dt = 100 A/µsec I_F = 10 A, di/dt = 100 A/µsec	t_{rr} I_{rm} Q_{rr}	— — —	400 27 5.5	600 — —	nsec A µC
Input Capacitance Output Capacitance Reverse Transfer Capacitance	V_{GS} = 0 V V_{DS} = 50 V f = 1 MHz	C_{iss} C_{oss} C_{rss}	— — —	2500 290 —	— — —	pF

CASE OUTLINE: TO-3 (/3)

PIN OUT:
PIN 1: GATE
PIN 2: SOURCE
CASE: DRAIN



NOTES:

1. THIS DIMENSION SHALL BE MEASURED AT POINTS .050" - .055" BELOW THE SEATING PLANE. WHEN GAGE IS NOT USED, MEASUREMENT WILL BE MADE AT SEATING PLANE.

THIS OUTLINE DOES NOT MEET THE MINIMUM CRITERIA ESTABLISHED BY JS-10 FOR REGISTRATION.