



PRELIMINARY

SFF9130-28D

SOLID STATE DEVICES, INC.

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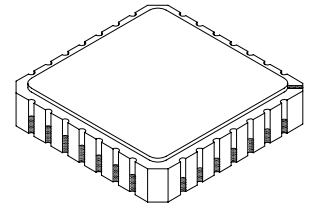
DESIGNER'S DATA SHEET

FEATURES:

- Rugged construction with poly silicon gate
- Low RDS (on) and high transconductance
- Excellent high temperature stability
- Very fast switching speed
- Fast recovery and superior dv/dt performance
- Increased reverse energy capability
- Low input transfer capacitance for easy paralleling
- Hermetically sealed surface mount package
- TX, TXV and Space Level screening available
- Replaces: 2x IRF9130 Types

-11 AMP
-100 VOLTS
0.30Ω
DUAL UNCOMMITTED
P-CHANNEL POWER MOSFET

28 PIN CLCC



MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	VALUE	UNIT
Drain to Source Voltage	V _{DS}	-100	Volts
Gate to Source Voltage	V _{GS}	±20	Volts
Continuous Drain Current T _C = 25°C T _C = 100°C	I _D	-11 -7	Amps
Operating and Storage Temperature	T _{op} & T _{stg}	-55 to +150	°C
Thermal Resistance, Junction to Case (Both)	R _{θJC}	3.5	°C/W
Total Device Dissipation T _C = 25°C T _C = 55°C	P _D	36 37	Watts
Single Pulse Avalange Energy	E _{AS}	84	mJ
Repetitive Avalange Energy	E _{AR}	7.5	mJ

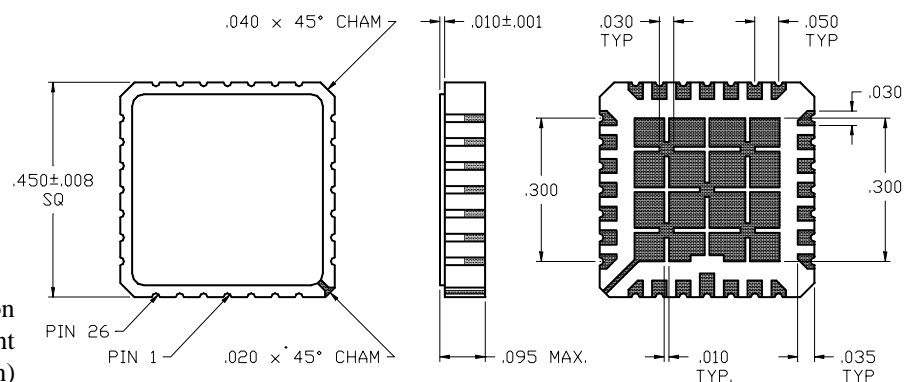
PACKAGE OUTLINE: 28 PIN CLCC

PIN OUT:

- SOURCE (1): 16 - 21**
DRAIN (1): 24 - 28
GATE (1): 22
SOURCE (2): 9 - 14
DRAIN (2): 2 - 6
GATE (2): 8

NOTE:

All drain/source pins must be connected on the PC board in order to maximize current carrying capability and to minimize RDS (on)



NOTE: All specifications are subject to change without notification. SCD's for these devices should be reviewed by SSDI prior to release.

DATA SHEET #: FP0035D

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ELECTRICAL CHARACTERISTICS @ T_J=25°C (Unless Otherwise Specified)

RATING	SYMBOL	MIN	TYP	MAX	UNIT	
Drain to Source Breakdown Voltage (V _{GS} = 0 V, I _D = 1mA)	BV_{DSS}	-100	-	-	V	
Temperature Coefficient of Breakdown Voltage	$\frac{\Delta BV_{DSS}}{\Delta T_J}$	-	0.87	-	V	
Drain to Source ON State Resistance ^{1/} (V _{GS} = -10 V)	R_{DS(on)}	-	-	0.30	Ω	
		I _D = 7A				
		I _D = 11A		0.35		
Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 250μA)	V_{GS(th)}	-2.0	-	-4.0	V	
Forward Transconductance (V _{DS} > I _{D(on)} x R _{DS(on)} Max, I _{DS} = 7A)	g_{fs}	3.0	5.0	-	S(Ω)	
Zero Gate Voltage Drain Current (V _{DS} = 80% rated V _{DS} , V _{GS} = 0 V, T _A = 25°C) (V _{DS} = 80% rated V _{DS} , V _{GS} = 0 V, T _A = 125°C)	I_{DSS}	-	-	-25	μA	
		-	-	250		
Gate to Source Leakage Forward Gate to Source Leakage Reverse	At rated V _{GS}	I_{GSS}	-	-	nA	
			-	-100		
			-	100		
Total Gate Charge Gate to Source Charge Gate to Drain Charge	V _{GS} = -10 Volts 50% rated V _{DS} I _D = -11A	Q_g Q_{gs} Q_{gd}	15 1 2	26 3 14	29 7.1 21	nC
Turn on Delay Time Rise Time Turn off DELAY Time Fall Time	V _{DD} = 50% of rated V _{DS} I _D = 11A R _G = 7.5Ω	t_{d(on)} t_r t_{d(off)} t_f	- - - -	15 10 30 12	60 140 140 140	nsec
Diode Forward Voltage (I _S = rated I _D , V _{GS} = 0V, T _J = 25°C)		V_{SD}	-	-	-4.7	V
Diode Reverse Recovery Time Reverse Recovery Charge	T _J = 25°C I _F = 10A di/dt = 100A/μsec	t_{rr} Q_{RR}	- -	125 -	250 3	nsec μC
Input Capacitance Output Capacitance Reverse Transfer Capacitance	V _{GS} = 0 Volts V _{DS} = -25 Volts f = 1 MHz	C_{iss} C_{oss} C_{rss}	- - -	860 350 125	- - -	pF

For thermal derating curves and other characteristic curves please contact SSDI Marketing Department.

NOTES:

- ^{1/} All package pins of the same terminations (Drain/Source/Gate) must be connected together to minimize R_{DS(on)} and maximize current carrying capability.