



PRELIMINARY

# SFF75N06-28

## SOLID STATE DEVICES, INC.

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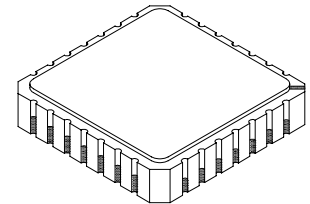
### DESIGNER'S DATA SHEET

#### FEATURES:

- Rugged construction with poly silicon gate
- Low RDS (on) and high transconductance
- Excellent high temperature stability
- Very fast switching speed
- Fast recovery and superior dv/dt performance
- Increased reverse energy capability
- Low input transfer capacitance for easy paralleling
- Hermetically sealed surface mount package
- TX, TXV and Space Level screening available

**30 AMP <sup>1/</sup>**  
**60 VOLTS**  
**25mΩ**  
**N-CHANNEL**  
**POWER MOSFET**

28 PIN CLCC



### MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	VALUE	UNIT
Drain to Source Voltage	V <sub>DS</sub>	100	Volts
Drain to Gate Voltage (RGS = 1.0 mΩ)	V <sub>DG</sub>	60	Volts
Gate to Source Voltage	V <sub>GS</sub>	±20	Volts
Continuous Drain Current @ TC = 25°C	I <sub>D</sub>	30	Amps
Operating and Storage Temperature	T <sub>op</sub> & T <sub>stg</sub>	-55 to +150	°C
Thermal Resistance, Junction to Case (All Four)	R <sub>θJC</sub>	3.5	°C/W
Total Device Dissipation @ TC = 25°C	P <sub>D</sub>	35	Watts

### PACKAGE OUTLINE: 28 PIN CLCC

#### PIN OUT:

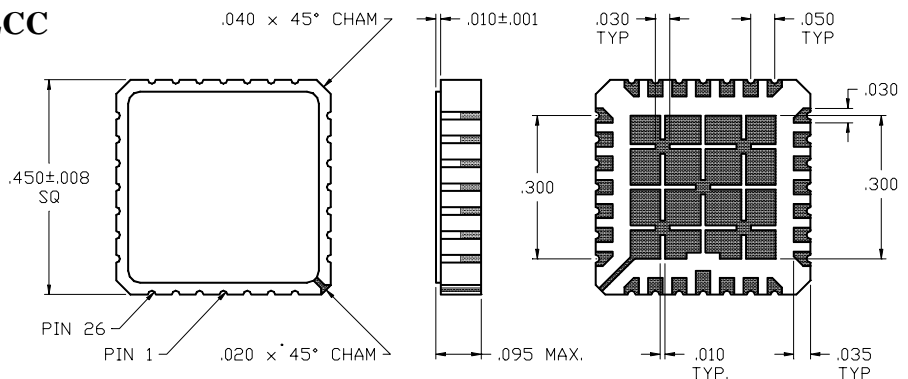
**SOURCE: 1, 15 - 28**

**DRAIN: 5 - 11**

**GATE: 2, 3, 13, 14**

#### NOTE:

All drain/source pins must be connected on the PC board in order to maximize current carrying capability and to minimize RDS (on)



NOTE: All specifications are subject to change without notification. SCD's for these devices should be reviewed by SSDI prior to release.

**DATA SHEET #: FT0001A**



**ELECTRICAL CHARACTERISTICS @ T<sub>J</sub> = 25°C (Unless Otherwise Specified)**

RATING	SYMBOL	MIN	TYP	MAX	UNIT
<b>Drain to Source Breakdown Voltage</b> (V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250μA)	<b>B<sub>V</sub>D<sub>SS</sub></b>	60	-	-	<b>V</b>
<b>Drain to Source ON State Resistance</b> <sup>2/</sup> (V <sub>GS</sub> = 10 V)	<b>R<sub>DS(on)</sub></b>	60% of Rated I <sub>D</sub> , T <sub>C</sub> = 25°C Rated I <sub>D</sub> , T <sub>C</sub> = 25°C 60% of Rated I <sub>D</sub> , T <sub>C</sub> = 150°C	- 23 25 27	25 27 -	<b>mΩ</b>
<b>Gate Threshold Voltage</b> (V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA)	<b>V<sub>GS(th)</sub></b>	2	-	4	<b>V</b>
<b>Forward Transconductance</b> (V <sub>DS</sub> > I <sub>D(on)</sub> x R <sub>DS(on)</sub> Max, I <sub>DS</sub> = 60% rated I <sub>D</sub> )	<b>g<sub>fs</sub></b>	15	35	-	<b>S(Ω)</b>
<b>Zero Gate Voltage Drain Current</b> (V <sub>DS</sub> = 80% rated V <sub>DS</sub> , V <sub>GS</sub> = 0 V, T <sub>A</sub> = 25°C) (V <sub>DS</sub> = 80% rated V <sub>DS</sub> , V <sub>GS</sub> = 0 V, T <sub>A</sub> = 125°C)	<b>I<sub>DSS</sub></b>	- -	- -	10 100	<b>μA</b>
<b>Gate to Source Leakage Forward</b> <b>Gate to Source Leakage Reverse</b>	At rated V <sub>GS</sub>	<b>I<sub>GSS</sub></b>	- -	- -	100 100 <b>nA</b>
<b>Total Gate Charge</b> <b>Gate to Source Charge</b> <b>Gate to Drain Charge</b>	V <sub>GS</sub> = 10 Volts 50% rated V <sub>DS</sub> Rated I <sub>D</sub>	<b>Q<sub>g</sub></b> <b>Q<sub>gs</sub></b> <b>Q<sub>gd</sub></b>	- - -	83 13 40	100 20 55 <b>nC</b>
<b>Turn on Delay Time</b> <b>Rise Time</b> <b>Turn off DELAY Time</b> <b>Fall Time</b>	V <sub>DD</sub> = 50% rated V <sub>DS</sub> rated I <sub>D</sub> R <sub>G</sub> = 6.2 Ω	<b>t<sub>d(on)</sub></b> <b>t<sub>r</sub></b> <b>t<sub>d(off)</sub></b> <b>t<sub>f</sub></b>	- - - -	20 35 65 40	40 70 130 80 <b>nsec</b>
<b>Diode Forward Voltage</b> (I <sub>S</sub> = rated I <sub>D</sub> , V <sub>GS</sub> = 0V, T <sub>J</sub> = 25°C)	<b>V<sub>SD</sub></b>	-	1.47	1.6	<b>V</b>
<b>Diode Reverse Recovery Time</b> <b>Reverse Recovery Charge</b>	T <sub>J</sub> = 25°C I <sub>F</sub> = 10A di/dt = 100A/μsec	<b>t<sub>rr</sub></b>	-	70	150 <b>nsec</b>
<b>Input Capacitance</b> <b>Output Capacitance</b> <b>Reverse Transfer Capacitance</b>	V <sub>GS</sub> = 0 Volts V <sub>DS</sub> = 25 Volts f = 1 MHz	<b>C<sub>iss</sub></b> <b>C<sub>oss</sub></b> <b>C<sub>rss</sub></b>	- - -	2600 700 260	2900 1100 275 <b>pF</b>

For thermal derating curves and other characteristic curves please contact SSDI Marketing Department.

**NOTES:**

1/ Die Rating: 75Amps.

2/ All package pins of the same terminations (Drain/Source/Gate) must be connected together to minimize R<sub>DS(on)</sub> and maximize current carrying capability.