



Solid State Devices, Inc.

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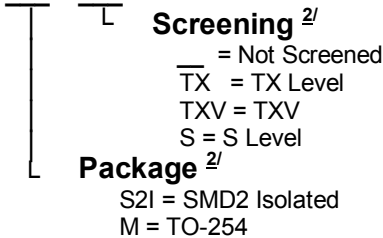
SFF25P20 Series

**25 AMP / 200 Volts
 150 mΩ typical
 P-Channel MOSFET**

DESIGNER'S DATA SHEET

Part Number/Ordering Information ^{1/}

SFF25P20



Features:

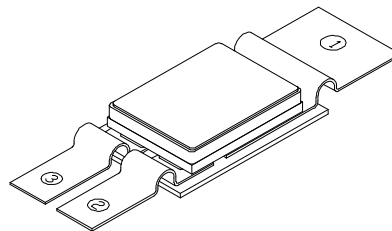
- polySi gate cell structure
- Low ON-resistance
- UIS (unclamped inductive switching) rated
- Hermetically Sealed, Isolated Package
- Low package inductance
- Stress relief provided by flexible leads – several options available
- Improved ($R_{DS(ON)}$ Q_G) figure of merit
- TX, TXV, S-Level screening available

Maximum Ratings		Symbol	Value	Units
Drain - Source Voltage		V_{DSS}	-200	V
Gate – Source Voltage	Continuous transient	V_{GS}	± 20 ± 30	V
Max. Continuous Drain Current	@ $T_c = 25^\circ C$	I_{D1}	25	A
Max. Instantaneous Drain Current (Tj limited)	@ $T_c = 25^\circ C$	I_{D3}	95	A
Max. Avalanche current		I_{AR}	25	A
Repetitive Avalanche Energy		E_{AR}	30	mJ
Total Power Dissipation	@ $T_c = 25^\circ C$	P_D	250	W
Operating & Storage Temperature		T_{OP} & T_{STG}	-55 to +150	$^\circ C$
Maximum Thermal Resistance	Junction to Case	$R_{\theta JC}$	0.83 0.6 typical	$^\circ C/W$

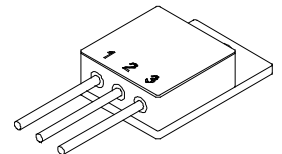
NOTES:

- ^{1/} For ordering information, price, operating curves, and availability- Contact factory.
- ^{2/} Screening based on MIL-PRF-19500. Screening flows available on request.
- ^{3/} Unless otherwise specified, all electrical characteristics @25°C.

SMD 2 Isolated



TO-254



NOTE: SEE DASH# DEFINITION TABLE FOR AVAILABLE LEAD FORMING CONFIGURATION

NOTE: All specifications are subject to change without notification. SCD's for these devices should be reviewed by SSDI prior to release.

DATA SHEET #: FT0009B

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SFF25P20 series

Electrical Characteristics (@25°C, unless otherwise specified)		Symbol	Min	Typ	Max	Units
Drain to Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	BV_{DSS}	200	—	—	V
Drain to Source On State Resistance	$V_{GS} = 10V, I_D = 12A, T_j = 25^\circ C$ $V_{GS} = 10V, I_D = 25A, T_j = 25^\circ C$	$R_{DS(on)}$	— —	125 150	150 —	mΩ
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	$V_{GS(th)}$	3.0	—	5.0	V
Gate to Source Leakage	$V_{GS} = \pm 20V$	I_{GSS}	—	—	±100	nA
Zero Gate Voltage Drain Current	$V_{DS} = 160V, V_{GS} = 0V, T_j = 25^\circ C$ $V_{DS} = 160V, V_{GS} = 0V, T_j = 125^\circ C$	I_{DSS}	— —	— —	25 1	μA mA
Forward Transconductance	$V_{DS} = 10V, I_D = 24A, T_j = 25^\circ C$	g_{fs}	5	12	—	Mho
Total Gate Charge	$V_{GS} = 10V$	Q_g	—	150	—	nC
Gate to Source Charge	$V_{DS} = 100V$	Q_{gs}	—	35	—	
Gate to Drain Charge	$I_D = 12A$	Q_{gd}	—	70	—	
Turn on Delay Time	$V_{GS} = 10V$	$t_{d(on)}$	—	35	—	nsec
Rise Time	$V_{DS} = 100V$	t_r	—	30	—	
Turn off Delay Time	$I_D = 12A$	$t_{d(off)}$	—	70	—	
Fall Time	$R_G = 4.7\Omega$	t_f	—	30	—	
Diode Forward Voltage	$I_F = 25A, V_{GS} = 0V$	V_{SD}	—	2.0	3.0	V
Diode Reverse Recovery Time	$I_F = 24A, di/dt = 100A/\mu sec$	t_{rr}	—	250	—	nsec
Peak Reverse Recovery Current						
Reverse Recovery Charge						
Input Capacitance	$V_{GS} = 0V$	C_{iss}	—	4200	—	pF
Output Capacitance	$V_{DS} = 25V$	C_{oss}	—	850	—	
Reverse Transfer Capacitance	$f = 1 MHz$	C_{rss}	—	350	—	

NOTES: Pulse Test: Pulse Width = 300μsec, Duty Cycle = 2%.

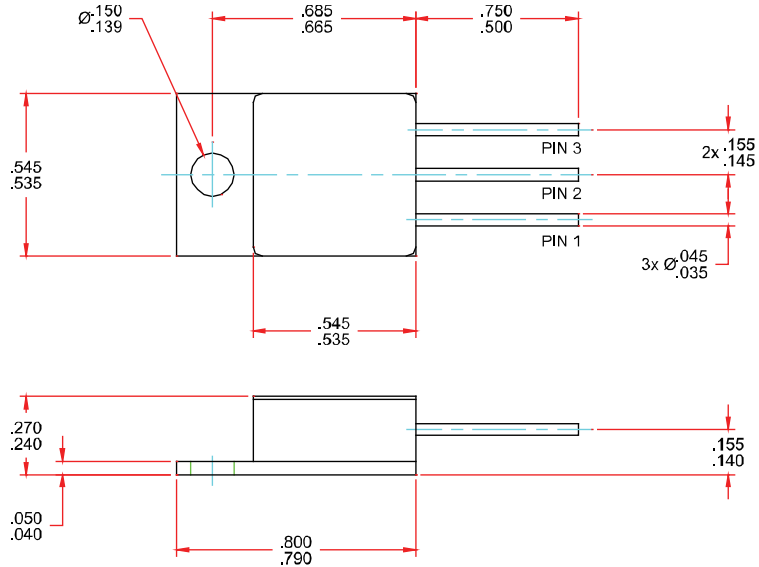


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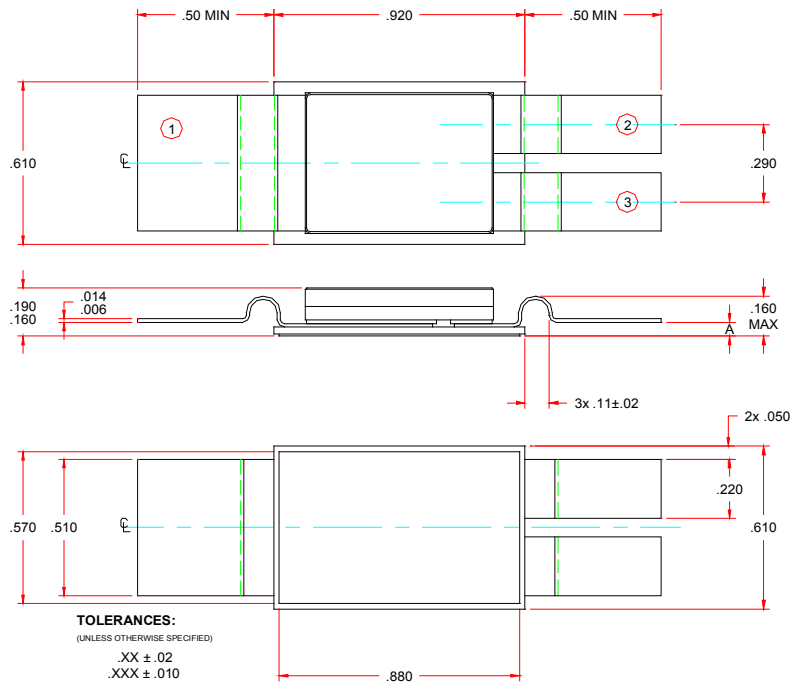
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SFF25P20 series

TO-254 (M)



SMD2 Isolated



LEAD FORMING CONFIGURATIONS			
SMD1I dash#	-01	-02	-03
A	0.062"	0.000"	0.097"

PIN ASSIGNMENT (Standard)			
Package	Drain	Source	Gate
SMD1I	Pin 1	Pin 2	Pin 3

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