



Solid State Devices, Inc.

14830 Valley View Blvd * La Mirada, Ca 90638

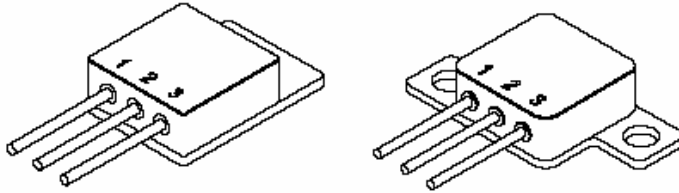
Phone: (562) 404-7855 * Fax: (562) 404-1773

ssdi@ssdi-power.com * www.ssdi-power.com

DESIGNER'S DATA SHEET

TO-254 and TO-254Z

Note 1: maximum current limited by package configuration



SFF75N08M
SFF75N08Z

55 AMP (note 1) /75 Volts
8.5 mO

N-Channel Trench Gate MOSFET

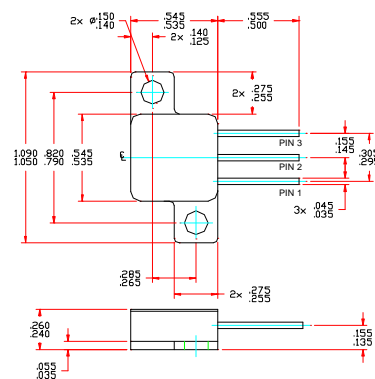
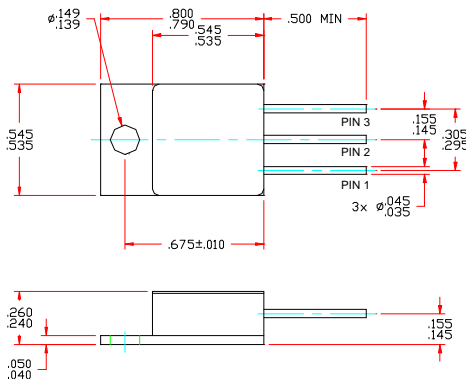
Features:

- Trench gate technology for high cell density
- Lowest ON-resistance in the industry
- Enhanced operating temperature range
- Hermetically Sealed, Isolated Package
- Low Total Gate Charge
- Fast Switching
- Enhanced replacement for IRF7MS2907
- TX, TXV, S-Level screening available
- Improved ($R_{DS(ON)}$ Q_G) figure of merit

Maximum Ratings		Symbol	Value	Units
Drain - Source Voltage		V_{DSS}	75	V
Gate - Source Voltage		V_{GS}	± 20	V
Max. Continuous Drain Current (package limited)	@ $T_C = 25^\circ C$	I_{D1}	55 (note 1)	A
	@ $T_C = 125^\circ C$	I_{D2}	55 (note 1)	A
Max. Instantaneous Drain Current (T_j limited)	@ $T_C = 25^\circ C$	I_{D3}	175	A
	@ $T_C = 125^\circ C$	I_{D4}	75	A
Max. Avalanche current	@ $L = 0.1$ mH	I_{AR}	75	A
Repetitive Avalanche Energy	@ $L = 0.1$ mH	E_{AR}	280	mJ
Total Power Dissipation	@ $T_C = 25^\circ C$	P_D	210	W
Operating & Storage Temperature		T_{OP} & T_{STG}	-55 to +175	$^\circ C$
Maximum Thermal Resistance (Junction to Case)		$R_{\theta JC}$	0.7 (typ 0.55)	$^\circ C/W$

TO-254 (M)

TO-254Z (Z)



NOTE: All specifications are subject to change without notification. SCD's for these devices should be reviewed by SSDI prior to release.

DATA SHEET #: FT0021A

DOC



Solid State Devices, Inc.

14830 Valley View Blvd * La Mirada, Ca 90638

Phone: (562) 404-7855 * Fax: (562) 404-1773

ssdi@ssdi-power.com * www.ssdi-power.com

SFF75N08M

SFF75N08Z

Electrical Characteristics ^{4/}		Symbol	Min	Typ	Max	Units
Drain to Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	BV_{DSS}	75	—	—	V
Drain to Source On State Resistance	$V_{GS} = 10V, I_D = 30A, T_j = 25^\circ C$ $V_{GS} = 10V, I_D = 30A, T_j = 125^\circ C$ $V_{GS} = 10V, I_D = 30A, T_j = 175^\circ C$	$R_{DS(on)}$	—	7.5 10.0 12.5	8.5 — —	mO
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	$V_{GS(th)}$	2.0	—	4.0	V
Gate to Source Leakage	$V_{GS} = \pm 20V$	I_{GSS}	—	—	± 100	nA
Zero Gate Voltage Drain Current	$V_{DS} = 60V, V_{GS} = 0V, T_j = 25^\circ C$ $V_{DS} = 60V, V_{GS} = 0V, T_j = 125^\circ C$ $V_{DS} = 60V, V_{GS} = 0V, T_j = 200^\circ C$	I_{DSS}	—	—	1 50 10	μA μA mA
Forward Transconductance	$V_{DS} = 15V, I_D = 30A, T_j = 25^\circ C$	g_{fs}	25	—	—	Mho
Total Gate Charge	$V_{GS} = 10V$	Q_g	—	150	220	nC
Gate to Source Charge	$V_{DS} = 35V$	Q_{gs}	—	35	—	
Gate to Drain Charge	$I_D = 110A$	Q_{gd}	—	50	—	
Turn on Delay Time	$V_{GS} = 10V$	$t_{d(on)}$	—	25	50	nsec
Rise Time	$V_{DS} = 35V$	t_r	—	210	300	
Turn off Delay Time	$I_D = 110A$	$t_{d(off)}$	—	70	125	
Fall Time	$R_G = 2.5O$	t_f	—	170	275	
Diode Forward Voltage	$I_F = 110A, V_{GS} = 0V$	V_{SD}	—	1.1	1.5	V
Diode Reverse Recovery Time	$I_F = 100A, di/dt = 100A/usec$	t_{rr}	—	85	135	nsec
Peak Reverse Recovery Current		$I_{RM(Rec)}$	—	4.5	7.5	A
Reverse Recovery Charge		Q_{rr}	—	0.16	0.35	μC
Input Capacitance	$V_{GS} = 0V$	C_{iss}	—	8000	—	pF
Output Capacitance	$V_{DS} = 25V$	C_{oss}	—	1000	—	
Reverse Transfer Capacitance	$f = 1 MHz$	C_{rss}	—	600	—	

NOTES:

* Pulse Test: Pulse Width = 300 μ sec, Duty Cycle = 2%.

1/ For Ordering Information, Price, and Availability Contact Factory.

2/ Screening per MIL-PRF-19500.

3/ For Package Outlines Contact Factory.

4/ Unless Otherwise Specified, All Electrical Characteristics @25°C.

Available Part Numbers:

Consult Factory

PIN ASSIGNMENT (Standard)

Package	Drain	Source	Gate
TO-254 (M)	Pin 1	Pin 2	Pin 3
TO-254Z (Z)	Pin 1	Pin 2	Pin 3

NOTE: All specifications are subject to change without notification. SCD's for these devices should be reviewed by SSDI prior to release.

DATA SHEET #: FT0021A

DOC