



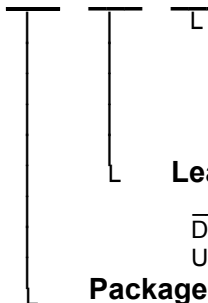
Solid State Devices, Inc.

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DESIGNER'S DATA SHEET

Part Number / Ordering Information ^{1/}

SFF50N30



Screening ^{2/}

— = Not Screened

TX = TX Level

TXV = TXV Level

S = S Level

Lead Option ^{3/}

— = Straight Leads

DB = Down Bend

UB = Up Bend

Package ^{3/ 4/}

M = TO-254

Z = TO-254Z

SFF50N30M
SFF50N30Z

50 AMP , 300 Volts, 55 mΩ
Avalanche Rated N-channel
MOSFET

Features:

- Rugged poly-Si gate
- Lowest ON-resistance in the industry
- Avalanche rated
- Hermetically Sealed, Isolated Package
- Low Total Gate Charge
- Fast Switching
- TX, TXV, S-Level screening available
- Improved ($R_{DS(ON)}$ Q_G) figure of merit

Maximum Ratings		Symbol	Value	Units
Drain - Source Voltage		V_{DSS}	300	V
Gate – Source Voltage	continuous	V_{GS}	± 20	V
	transient		± 30	
Max. Continuous Drain Current (package limited)	@ $T_C = 25^\circ C$	I_{D1}	50	A
Max. Instantaneous Drain Current (T_j limited)	@ $T_C = 25^\circ C$	I_{D2}	50	A
	@ $T_C = 125^\circ C$	I_{D3}	35	
Max. Avalanche current	@ $L = 0.1$ mH	I_{AR}	50	A
Single and Repetitive Avalanche Energy	@ $L = 0.1$ mH	E_{AS}	1500	mJ
		E_{AR}	50	
Total Power Dissipation	@ $T_C = 25^\circ C$	P_D	150	W
Operating & Storage Temperature		$T_{OP} \text{ \& } T_{STG}$	-55 to +150	$^\circ C$
Maximum Thermal Resistance (Junction to Case)		$R_{\theta JC}$	1.0 (typ.0.75)	$^\circ C / W$

NOTES:

*Pulse Test: Pulse Width = 300μsec, Duty Cycle = 2%.

1/ For ordering information, price, and availability - contact factory.

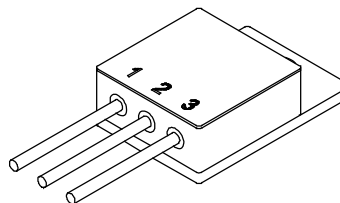
2/ Screening based on MIL-PRF-19500. Screening flows available on request.

3/ For package outlines / lead bending options / pinout configurations - contact factory.

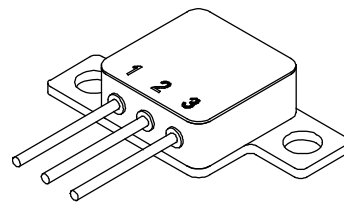
4/ Maximum current limited by package configuration

5/ Unless otherwise specified, all electrical characteristics @25°C.

TO-254



TO-254Z



NOTE: All specifications are subject to change without notification.
SCD's for these devices should be reviewed by SSDI prior to release.

DATA SHEET #: FT0038C

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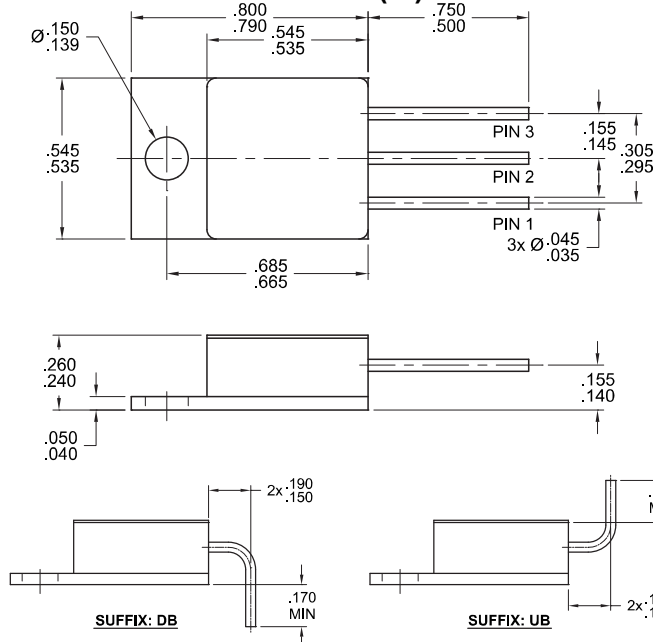
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SFF50N30M

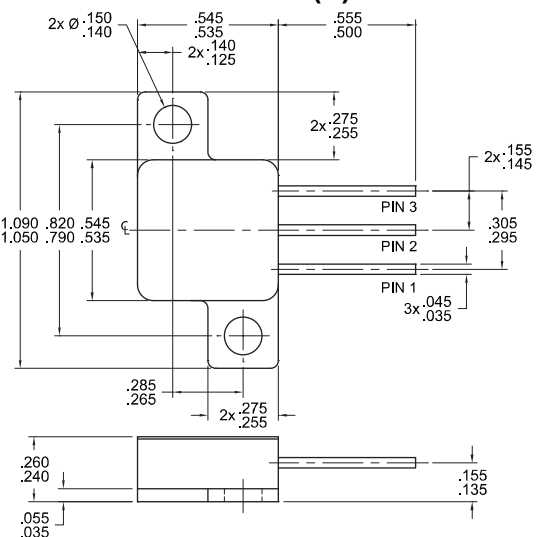
SFF50N30Z

Electrical Characteristics ^{5/}		Symbol	Min	Typ	Max	Units
Drain to Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	BV_{DSS}	300	310	—	V
Drain to Source On State Resistance	$V_{GS} = 10V, I_D = 35A, T_j = 25^\circ C$ $V_{GS} = 10V, I_D = 35A, T_j = 125^\circ C$	$R_{DS(on)}$	—	55 110	65 —	mΩ
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 1.0mA, T_j = 25^\circ C$ $V_{DS} = V_{GS}, I_D = 1.0mA, T_j = 125^\circ C$ $V_{DS} = V_{GS}, I_D = 1.0mA, T_j = -55^\circ C$	$V_{GS(th)}$	2.5 1.5 —	4.0 3.0 5.0	5.0 — 6	V
Gate to Source Leakage	$V_{GS} = \pm 20V, T_j = 25^\circ C$ $V_{GS} = \pm 20V, T_j = 125^\circ C$	I_{GSS}	— —	10 30	± 100 —	nA
Zero Gate Voltage Drain Current	$V_{DS} = 300V, V_{GS} = 0V, T_j = 25^\circ C$ $V_{DS} = 300V, V_{GS} = 0V, T_j = 125^\circ C$	I_{DSS}	— —	0.01 5.0	25 250	μA μA
Forward Transconductance	$V_{DS} = 10V, I_D = 35A, T_j = 25^\circ C$	g_{fs}	20	33	—	Mho
Total Gate Charge	$V_{GS} = 10V$	Q_g	—	140	250	nC
Gate to Source Charge	$V_{DS} = 150V$	Q_{gs}	—	50	—	
Gate to Drain Charge	$I_D = 35A$	Q_{gd}	—	60	—	
Turn on Delay Time	$V_{GS} = 10V$	$t_{d(on)}$	—	40	50	nsec
Rise Time	$V_{DS} = 150V$	t_r	—	40	50	
Turn off Delay Time	$I_D = 50A$	$t_{d(off)}$	—	110	125	
Fall Time	$R_G = 4.0\Omega, pw = 3\mu s$	t_f	—	40	50	
Diode Forward Voltage	$I_F = 50A, V_{GS} = 0V$	V_{SD}	—	0.95	1.5	V
Diode Reverse Recovery Time	$I_F = 10A, di/dt = 100A/\mu sec$	t_{rr}	—	180	200	nsec
Reverse Recovery Charge		Q_{rr}	—	1.3	—	μC
Input Capacitance	$V_{GS} = 0V$	C_{iss}	—	5000	—	pF
Output Capacitance	$V_{DS} = 25V$	C_{oss}	—	750	—	
Reverse Transfer Capacitance	$f = 1 MHz$	C_{rss}	—	145	—	

TO-254 (M)



TO-254Z (Z)



PIN ASSIGNMENT (Standard)

Package	Drain	Source	Gate
TO-254 (M)	Pin 1	Pin 2	Pin 3
TO-254Z (Z)	Pin 1	Pin 2	Pin 3

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