Solid State Devices, Inc.
14701 Firestone Blvd * La Mirada, Ca 90638
Phone: (562) 404-4474 * Fax: (562) 404-1773
ssdi@ssdi-power.com * www.ssdi-power.com

SFF3810 Series

350 AMP , 75 Volts, 2.5 mΩ Avalanche Rated N-channel TrenchFET

DESIGNER'S DATA SHEET

Part Number / Ordering Information [1/]

SFF3810 ___ ___ ___

Screening [2/]
__ = Not Screened
TX = TX Level
TXV = TXV Level
S = S Level

Lead Option [3/]
__ = Straight Leads
DB = Down Bend
UB = Up Bend

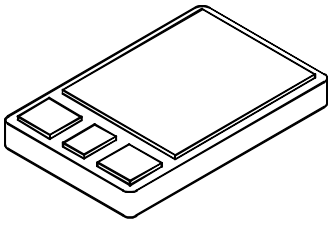
Package [3/ 4/]
Q = TO-258 modified
E = MILPACK III

Features:
- Rugged poly-Si gate
- Lowest ON-resistance in the industry
- Avalanche rated
- Hermetically Sealed, Isolated Package
- Low Total Gate Charge
- Fast Switching
- TX, TXV, S-Level screening available
- Improved ($R_{DS(ON)}$ Q_G) figure of merit

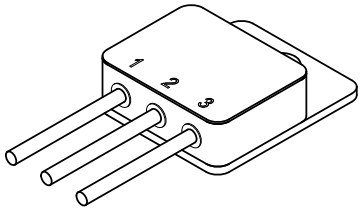
Maximum Ratings [5/]		Symbol	Value	Units
Drain - Source Voltage		V_{DSS}	75	V
Gate – Source Voltage	continuous transient	V_{GS}	± 20 ± 30	V
Max. Continuous Drain Current (package limited)	@ T_C = 25ºC	I_{D1}	60	A
Max. Instantaneous Drain Current (Tj limited)	@ T_C = 25ºC @ T_C = 125ºC	I_{D2} I_{D3}	350 150	A
Max. Avalanche current	@ L= 0.1 mH	I_{AR}	200	A
Single and Repetitive Avalanche Energy	@ L= 0.1 mH	E_{AS}	3000	mJ
Total Power Dissipation	@ T_C = 25ºC	P_D	600	W
Operating & Storage Temperature		T_{OP} & T_{STG}	-55 to 175	ºC
Maximum Thermal Resistance (Junction to Case)		$R_{\theta JC}$	0.5	ºC/W

NOTES:
*Pulse Test: Pulse Width = 300µsec, Duty Cycle = 2%.
1/ For ordering information, price, and availability - contact factory.
2/ Screening based on MIL-PRF-19500. Screening flows available on request.
3/ For lead bending options / pinout configurations - contact factory.
4/ Maximum current limited by package configuration
5/ Unless otherwise specified, all electrical characteristics @25°C.

MILPACK III (E)



TO-258 modified (Q)



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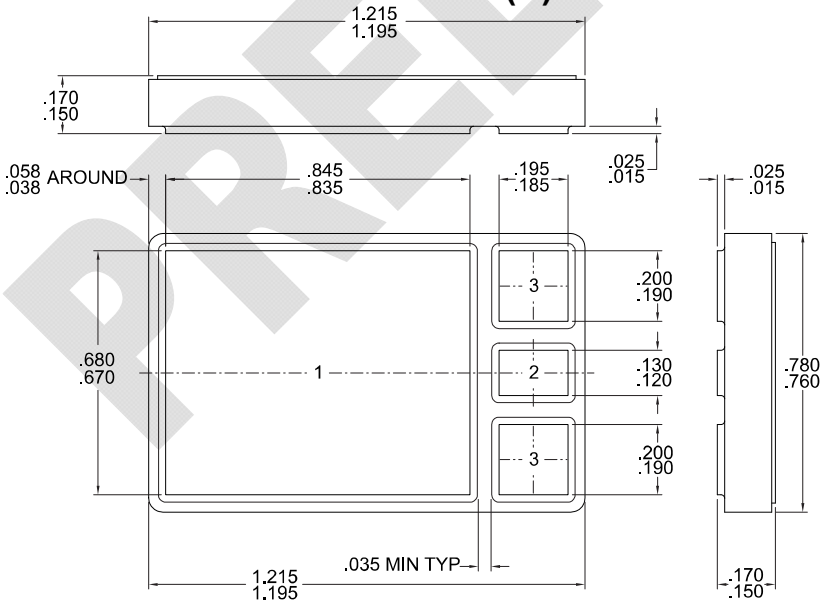
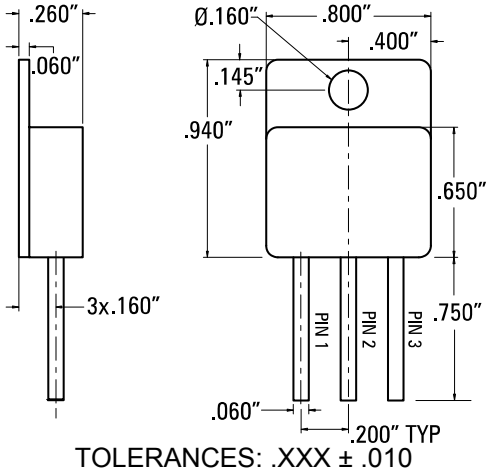
Electrical Characteristics[5/]		Symbol	Min	Typ	Max	Units
Drain to Source Breakdown Voltage	V_{GS} = 0V, I_D = 3 mA	BV_{DSS}	75	80	—	V
Drain to Source On State Resistance	V_{GS} = 10V, I_D = 125A, Tj= 25°C	$R_{DS(on)}$	—	2.5	3	mΩ
	V_{GS} = 15V, I_D = 125A, Tj=25°C		—	2	-	
	V_{GS} = 10V, I_D = 125A, Tj= 175°C		—	5	—	
Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 8.0mA, Tj= 25°C	$V_{GS(th)}$	2.5	3.6	5.0	V
	V_{DS} = V_{GS}, I_D = 8.0mA, Tj= 125°C		1.5	3.0	—	
	V_{DS} = V_{GS}, I_D = 8.0mA, Tj= -55°C		—	5	6	
Gate to Source Leakage	V_{GS} = ±20V, Tj= 25°C	I_{GSS}	—	10	±200	nA
	V_{GS} = ±20V, Tj= 125°C		—	30	—	
Zero Gate Voltage Drain Current	V_{DS} = 75V, V_{GS} = 0V, T_j = 25°C	I_{DSS}	—	0.06	25	µA
	V_{DS} = 75V, V_{GS} = 0V, T_j = 150°C		—	150	2000	µA
Forward Transconductance	V_{DS} = 10V, I_D = 60A, T_j = 25°C	g_{fs}	65	100	—	Mho
Total Gate Charge	V_{GS} = 10V	Q_g	—	550	—	nC
Gate to Source Charge	V_{DS} = 37.5V	Q_{gs}	—	180	—	
Gate to Drain Charge	I_D = 200A	Q_{gd}	—	140	—	
Turn on Delay Time	V_{GS} = 10V	$t_{d(on)}$	—	50	—	nsec
Rise Time	V_{DS} = 37.5V	t_r	—	40	—	
Turn off Delay Time	I_D = 200A	$t_{d(off)}$	—	80	—	
Fall Time	R_G = 1.0Ω, pw= 3us	t_f	—	40	—	
Diode Forward Voltage	I_F = 100A, V_{GS} = 0V	V_{SD}	—	0.90	1.25	V
Diode Reverse Recovery Time	I_F = 150A, di/dt = 100A/usec	t_{rr1}	—	150	—	nsec
Reverse Recovery Charge		I_{rm1}	—	7	—	A
		Q_{rr1}	—	360	—	nC
Input Capacitance	V_{GS} = 0V	C_{iss}	—	41	—	nF
Output Capacitance	V_{DS} = 25V	C_{oss}	—	4.15	—	nF
Reverse Transfer Capacitance	f = 1 MHz	C_{rss}	—	530	—	pF

MILPACK III (E)



TO-258 mod (Q)



TOLERANCES: .XXX ± .010

PIN ASSIGNMENT (Standard)

Package	Drain	Source	Gate
TO-258 mod	Pin 1	Pin 2	Pin 3
MILPACK III	Pin 1	Pin 2	Pin 3

NOTE: All specifications are subject to change without notification.
SCD's for these devices should be reviewed by SSDI prior to release.

DATA SHEET #: FT0051A | **DOC**