



Solid State Devices, Inc.

14701 Firestone Blvd * La Mirada, CA 90638
 Phone: (562) 404-4474 * Fax: (562) 404-1773
 ssdi@ssdi-power.com * www.ssdi-power.com

DESIGNER'S DATA SHEET

Part Number / Ordering Information ^{1/}

SFL630

J

L

Screening ^{2/}

___ = Not Screened
 TX = TX Level
 TXV = TXV Level
 S = S Level

Lead Options

(for TO-257 package)

___ = Straight Leads
 DB = Down Bend
 UB = Up Bend

Package

J = TO-257
 S.5 = SMD.5
 G = Cerpack

SFL630 Series

Logic Level

**10 AMP, 200 Volts, 400 mΩ
 Avalanche Rated N-MOSFET**

Features:

- Rugged Technology
- Very Low ON-Resistance: 200 mΩ typ
- Avalanche Rated
- Hermetically Sealed Power Packaging
- Low Total Gate Charge, Fast Switching
- Enhanced Performance Replacement for IRL630 Types and 2N6904
- TX, TXV, and S-Level Screening Available

Maximum Ratings ^{3/}	Symbol	Value	Unit
Drain – Source Voltage	V_{DSS}	200	V
Gate – Source Voltage, Continuous	V_{GS}	±10	V
Gate – Source Voltage, Transient		±15	V
Max. Continuous Drain Current (package limited)	I_{D1} I_{D2}	10 6	A
Max. Avalanche Current	I_{AR}	10	A
Single Pulse Avalanche Energy	E_{AS}	250	mJ
Total Power Dissipation @ $T_C = 25^\circ C$	P_D	120 150	W
Operating & Storage Temperature	T_{OP} & T_{STG}	-55 to +175	°C
Maximum Thermal Resistance (Junction to Case)	$R_{\theta JC}$	3.5 1.70	°C/W

NOTES:

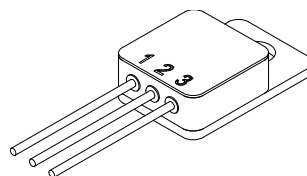
*Pulse Test: Pulse Width = 300 μsec, Duty Cycle = 2%.

^{1/} For ordering information, price, and availability - contact factory.

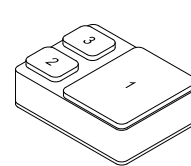
^{2/} Screening based on MIL-PRF-19500. Screening flows available on request.

^{3/} Unless otherwise specified, all electrical characteristics @25°C.

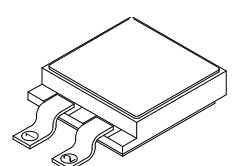
TO-257 (J)



SMD.5 (S.5)



Cerpack (G)



NOTE: All specifications are subject to change without notification.
 SCD's for these devices should be reviewed by SSDI prior to release.

DATA SHEET #: FT0057B

DOCX



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SFL630 Series

Electrical Characteristics ^{3/}		Symbol	Min	Typ	Max	Unit
Drain to Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 0.25\text{ mA}$	BV_{DSS}	200	225	-	V
Drain to Source On State Resistance	$V_{GS} = 5\text{ V}, I_D = 5\text{ A}, T_J = 25^\circ\text{C}$	$R_{DS(on)}$	-	200	400	mΩ
	$V_{GS} = 5\text{ V}, I_D = 10\text{ A}, T_J = 25^\circ\text{C}$		-	250	500	
	$V_{GS} = 4\text{ V}, I_D = 5\text{ A}, T_J = 25^\circ\text{C}$		-	200	-	
	$V_{GS} = 5\text{ V}, I_D = 10\text{ A}, T_J = 125^\circ\text{C}$		-	400	-	
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 1\text{ mA}, T_J = 25^\circ\text{C}$	$V_{GS(th)}$	1.0	1.6	2.0	V
	$V_{DS} = V_{GS}, I_D = 1\text{ mA}, T_J = 125^\circ\text{C}$		0.5	1.0	-	
	$V_{DS} = V_{GS}, I_D = 1\text{ mA}, T_J = -55^\circ\text{C}$		-	2.0	3.0	
Gate to Source Leakage	$V_{GS} = \pm 10\text{ V}, T_J = 25^\circ\text{C}$	I_{GSS}	-	1	±100	nA
	$V_{GS} = \pm 10\text{ V}, T_J = 125^\circ\text{C}$		-	10	±200	
Zero Gate Voltage Drain Current	$V_{DS} = 200\text{ V}, V_{GS} = 0\text{ V}, T_J = 25^\circ\text{C}$	I_{DSS}	-	0.01	1	μA
	$V_{DS} = 160\text{ V}, V_{GS} = 0\text{ V}, T_J = 125^\circ\text{C}$		-	100	250	
Forward Transconductance	$V_{DS} = 50\text{ V}, I_D = 5.4\text{ A}, T_J = 25^\circ\text{C}$	g_{fs}	3	6	-	Mho
Total Gate Charge	$V_{GS} = 10\text{ V}$	Q_g	-	42	70	nC
Gate to Source Charge	$V_{DS} = 100\text{ V}$	Q_{gs}	-	6	10	
Gate to Drain Charge	$I_D = 8\text{ A}$	Q_{gd}	-	15	24	
Turn on Delay Time	$V_{GS} = 10\text{ V}$	$t_{d(on)}$	-	7.5	15	nsec
Rise Time	$V_{DS} = 100\text{ V}$	t_r	-	15	30	
Turn off Delay Time	$I_D = 9\text{ A}$	$t_{d(off)}$	-	75	110	
Fall Time	$R_G = 6\text{ }\Omega$	t_f	-	30	45	
Diode Forward Voltage	$I_F = 10\text{ A}, V_{GS} = 0\text{ V}$	V_{SD}	-	0.85	2.0	V
Diode Reverse Recovery Time	$I_F = 9\text{ A}, di/dt = 100\text{ A}/\mu\text{sec}$	t_{rr}	-	190	350	nsec
Peak Reverse Recovery Current		Q_{rr}	-	1	-	
Reverse Recovery Charge						μC
Input Capacitance	$V_{GS} = 0\text{ V}$	C_{iss}	-	1100	-	pF
Output Capacitance	$V_{DS} = 25\text{ V}$	C_{oss}	-	450	-	
Reverse Transfer Capacitance	$f = 1\text{ MHz}$	C_{rss}	-	60	-	

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SFL630 series

PACKAGE OUTLINE:

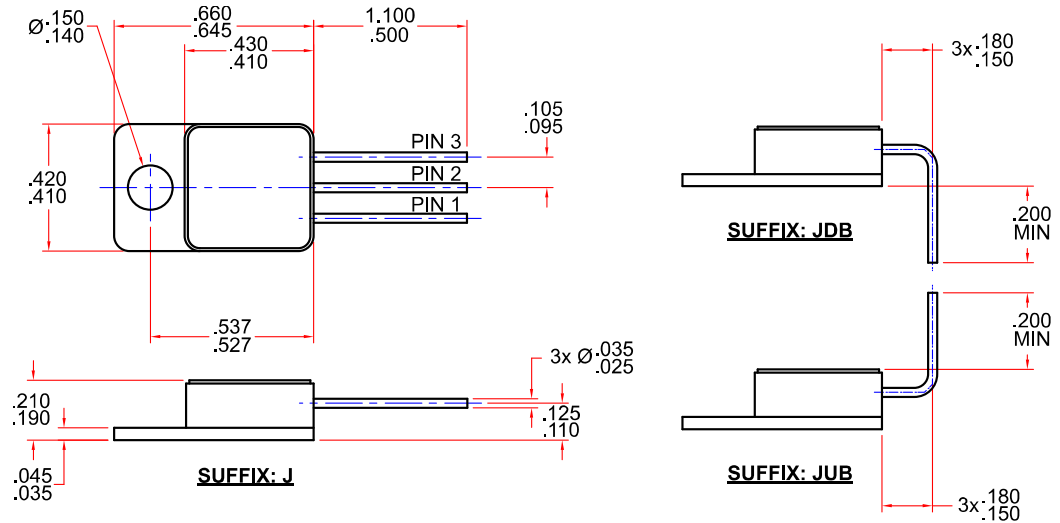
TO-257 (J)

PINOUT:

PIN 1: DRAIN

PIN 2: SOURCE

PIN 3: GATE



PACKAGE OUTLINE:

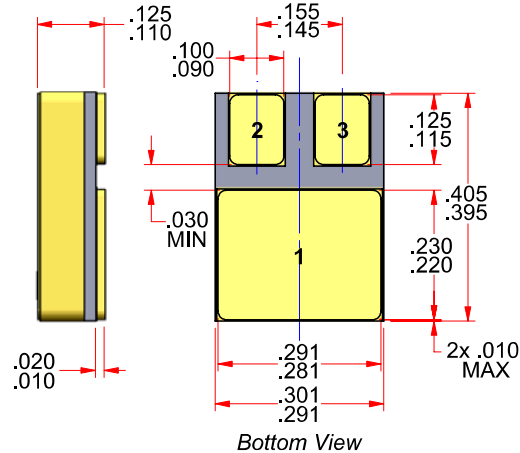
SMD.5 (S.5)

PINOUT:

PIN 1: DRAIN

PIN 2: SOURCE

PIN 3: GATE



PACKAGE OUTLINE:

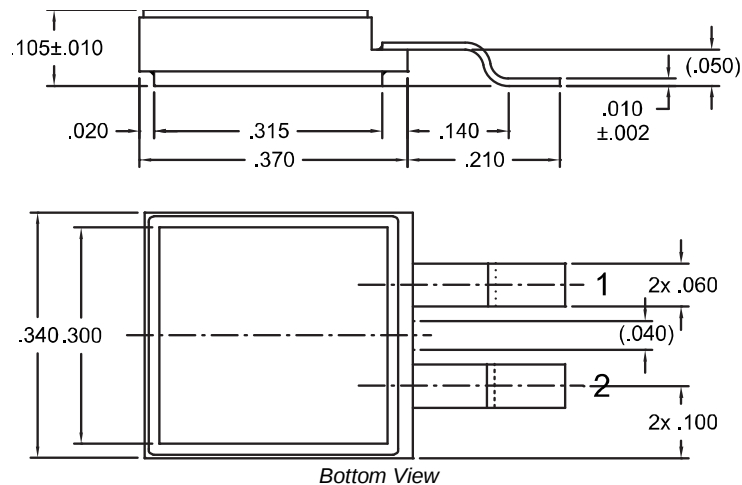
Cerpack (G)

PINOUT:

PIN 1: DRAIN

PIN 2: SOURCE

BOTTOM PAD: GATE



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