



Solid State Devices, Inc.

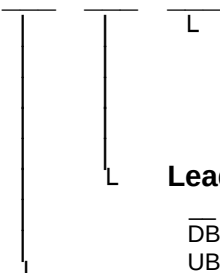
14701 Firestone Blvd * La Mirada, Ca 90638
Phone: (562) 404-4474 * Fax: (562) 404-1773
ssdi@ssdi-power.com * www.ssdi-power.com

SFF55N70 - SFF70N70 Series

DESIGNER'S DATA SHEET

Part Number / Ordering Information ^{1/}

SFF70N70



Screening ^{2/}

— = Not Screened
TX = TX Level
TXV = TXV Level
S = S Level

Lead Option ^{3/}

— = Straight Leads
DB = Down Bend
UB = Up Bend

Package ^{3/ 4/}

S2 = SMD2

N = TO-258
P = TO-259

**55 - 70 AMP , 700 Volts, 50 mΩ
Avalanche Rated N-Channel
MOSFET**

Features:

- Rugged Poly-Si Gate
- Lowest ON-Resistance in the Industry
- Avalanche Rated
- Hermetically Sealed, Isolated Package
- Low Total Gate Charge
- Fast Switching
- TX, TXV, and S-Level Screening Available
- Improved ($R_{DS(ON)}$ Q_G) Figure of Merit

Maximum Ratings ^{5/}	Symbol	Value	Unit
Drain - Source Voltage	V_{DS}	700	V
Gate - Source Voltage	V_{GS}	± 20 ± 30	V
Continuous Drain Current (T_{OP} limited) @ $T_C = 25^\circ C$	I_{D1} ^{6/} I_{D2}	55 70	A
Continuous Drain Current (T_{OP} limited) @ $T_C = 100^\circ C$	I_{D3}	44	A
Pulsed Drain Current (P_{width}/T_{OP} limited) @ $T_C = 25^\circ C$	I_{D4}	220	A
Single and Repetitive Avalanche Energy @ $L = 0.1$ mH	E_{AS} E_{AR}	2000 3	mJ
Total Power Dissipation @ $T_C = 25^\circ C$	P_D	500	W
Operating & Storage Temperature	T_{OP} & T_{STG}	-55 to +150	$^\circ C$
Maximum Thermal Resistance (Junction to Case)	$R_{\theta JC}$	0.25	$^\circ C/W$

NOTES:

*Pulse Test: Pulse Width = 300 μ sec, Duty Cycle = 2%.

^{1/} For ordering information, price, and availability - contact factory.

^{2/} Screening based on MIL-PRF-19500. Screening flows available on request.

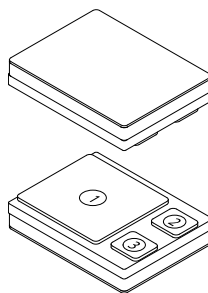
^{3/} For lead bending options / pinout configurations - contact factory.

^{4/} Maximum current limited by package configuration

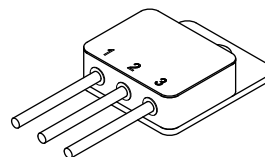
^{5/} Unless otherwise specified, all electrical characteristics @ $25^\circ C$.

^{6/} Package limited.

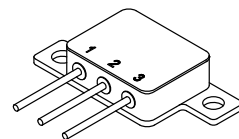
SMD2 (S2)



TO-258 (N)



TO-259 (P)



NOTE: All specifications are subject to change without notification.
SCD's for these devices should be reviewed by SSDI prior to release.

DATA SHEET #: FT0061D

DOCX



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Electrical Characteristics ^{5/}		Symbol	Min	Typ	Max	Unit
Drain to Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$	BV_{DSS}	700	740	—	V
Drain to Source On State Resistance	$V_{GS} = 10\text{ V}, I_D = 40\text{ A}, T_J = 25^\circ\text{C}$ $V_{GS} = 10\text{ V}, I_D = 40\text{ A}, T_J = 125^\circ\text{C}$	$R_{DS(on)}$	— —	40 80	50 —	mΩ
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 3.5\text{ mA}, T_J = 25^\circ\text{C}$ $V_{DS} = V_{GS}, I_D = 3.5\text{ mA}, T_J = 125^\circ\text{C}$ $V_{DS} = V_{GS}, I_D = 3.5\text{ mA}, T_J = -55^\circ\text{C}$	$V_{GS(th)}$	3.5 2.5 —	4.2 3.5 5	4.5 — 5.5	V
Gate to Source Leakage	$V_{GS} = \pm 20\text{ V}, T_J = 25^\circ\text{C}$ $V_{GS} = \pm 20\text{ V}, T_J = 125^\circ\text{C}$	I_{GSS}	— —	20 50	± 200 —	nA
Zero Gate Voltage Drain Current	$V_{DS} = 650\text{ V}, V_{GS} = 0\text{ V}, T_J = 25^\circ\text{C}$ $V_{DS} = 650\text{ V}, V_{GS} = 0\text{ V}, T_J = 125^\circ\text{C}$	I_{DSS}	— —	1 10	50 300	μA μA
Total Gate Charge	$V_{GS} = 10\text{ V}$	Q_g	—	350	450	nC
Gate to Source Charge	$V_{DS} = 480\text{ V}$	Q_{gs}	—	70	150	
Gate to Drain Charge	$I_D = 55\text{ A}$	Q_{gd}	—	200	350	
Turn on Delay Time	$V_{GS} = 13\text{ V}$	$t_{d(on)}$	—	50	100	nsec
Rise Time	$V_{DS} = 400\text{ V}$	t_r	—	20	40	
Turn off Delay Time	$I_D = 55\text{ A}$	$t_{d(off)}$	—	200	300	
Fall Time	$R_G = 1.8\ \Omega, pw = 3\ \mu\text{s}$	t_f	—	20	40	
Diode Forward Voltage	$I_F = 27\text{ A}, V_{GS} = 0\text{ V}$	V_{SD}	—	1.0	1.2	V
Diode Reverse Recovery Time	$I_F = 10\text{ A}, di/dt = 100\text{ A}/\mu\text{sec}$	t_{rr}	—	180	250	nsec
Reverse Recovery Charge	$I_F = 10\text{ A}, di/dt = 100\text{ A}/\mu\text{sec}$	I_{rm}	—	—	—	A
	$I_F = 10\text{ A}, di/dt = 100\text{ A}/\mu\text{sec}$	Q_{rr}	—	—	—	μC
Input Capacitance	$V_{GS} = 0\text{ V}$	C_{iss}	—	10,000	—	pF
Output Capacitance	$V_{DS} = 100\text{ V}$	C_{oss}	—	450	—	
Reverse Transfer Capacitance	$f = 1\text{ MHz}$	C_{rss}	—	40	—	

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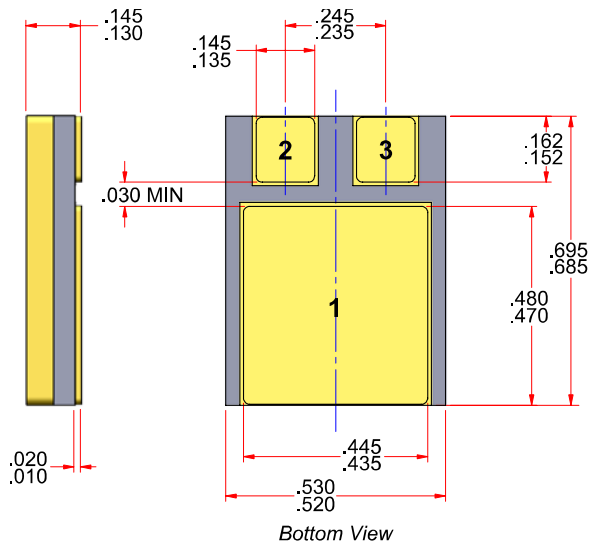


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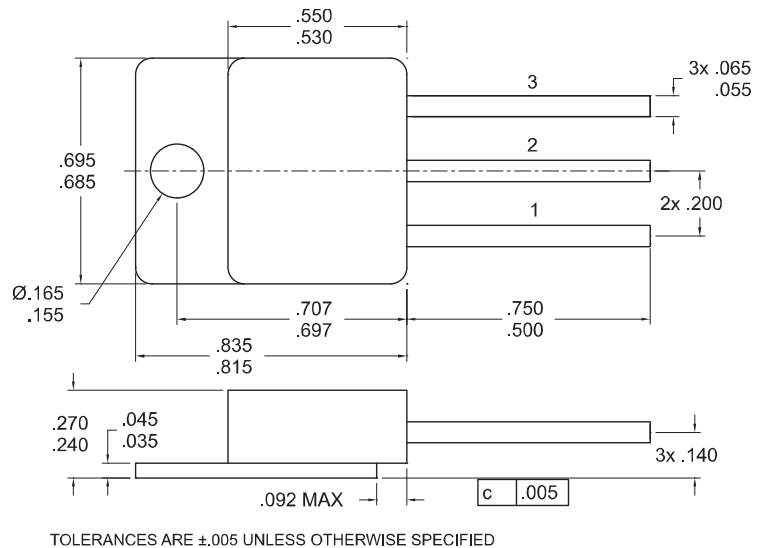
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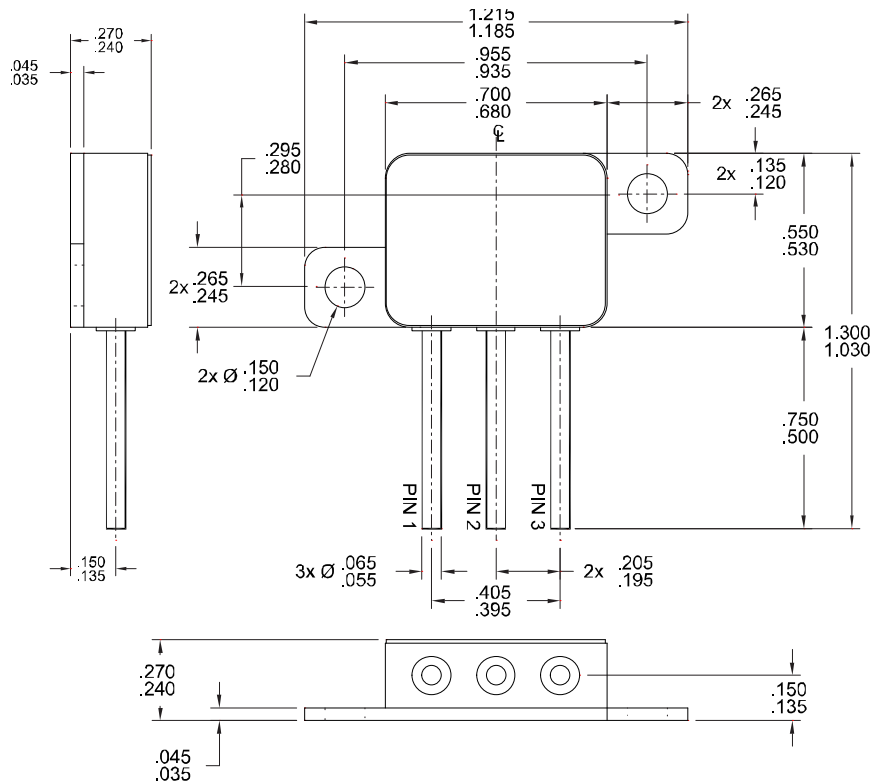
SMD2 (S2)



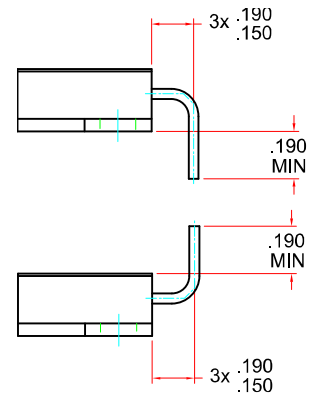
TO-258 (N)



TO-259 (P)



**Lead Bend Options
for TO-258 (N) and TO-259 (P)**



PIN ASSIGNMENT (Standard)

Package	Drain	Source	Gate
SMD2 (S2)	Pin 1	Pin 2	Pin 3
TO-258 (N)	Pin 1	Pin 2	Pin 3
TO-259 (P)	Pin 1	Pin 2	Pin 3

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