



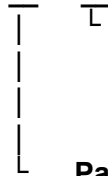
Solid State Devices, Inc.

14701 Firestone Blvd * La Mirada, CA 90638
 Phone: (562) 404-4474 * Fax: (562) 404-1773
 ssdi@ssdi-power.com * www.ssdi-power.com

DESIGNER'S DATA SHEET

Part Number / Ordering Information ^{1/}

SFF110P20



Screening ^{2/}

- = Not Screened
- TX = TX Level
- TXV = TXV Level
- S = S Level

Package

FP5 = 5 Pin Flat Pack

SFF110P20FP5

**100 AMP
 Avalanche Rated
 P-channel MOSFET
 200 Volts, 30 mΩ**

Features:

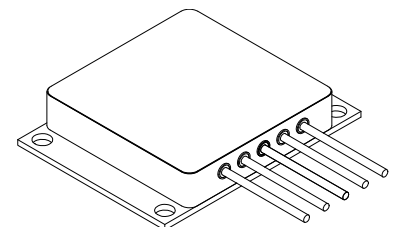
- TrenchMOS technology
- Lowest ON-resistance in the industry
- Avalanche rated
- Hermetically Sealed, Hot Case power SMD
- Low Total Gate Charge
- Fast Switching
- TX, TXV, S-Level screening available ^{2/}
- Improved ($R_{DS(ON)}$, Q_G) figure of merit

Maximum Ratings		Symbol	Value	Units
Drain – Source Voltage		V_{DSS}	200	V
Gate – Source Voltage	Continuous Transient	V_{GS}	± 15 ± 25	V
Max. Continuous Drain Current (package limited)	@ $T_C = 25^\circ C$	I_{D1}	110	A
Source Current (Tj limited)	@ $T_C = 25^\circ C$	I_S	350	A
Avalanche Energy		E_{AS}	3	J
Total Power Dissipation	@ $T_C = 25^\circ C$	P_D	830	W
Operating & Storage Temperature		T_{OP} & T_{STG}	-55 to +150	$^\circ C$
Maximum Thermal Resistance	Junction to Case Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	0.15 20	$^\circ C/W$

NOTES:

- ^{1/} For ordering information, price, and availability - contact factory.
- ^{2/} Screening based on MIL-PRF-19500. Screening flows available on request.
- ^{3/} Unless otherwise specified, all electrical characteristics @25 $^\circ C$.

5 Pin Flat Pack (FP5)



NOTE: All specifications are subject to change without notification.
 SCD's for these devices should be reviewed by SSDI prior to release.

DATA SHEET #: FT0067A

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SFF110P20FP5

Electrical Characteristics ^{3/}		Symbol	Min	Typ	Max	Units
Drain to Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 0.25\text{ mA}$	BV_{DSS}	200	240	—	V
Drain to Source On State Resistance	$V_{GS} = 10\text{ V}, I_D = 60\text{ A}, T_J = 25^\circ\text{C}$	$R_{DS(on)}$	—	25	35	mΩ
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}, T_J = 25^\circ\text{C}$	$V_{GS(th)}$	2.5	3.2	4.5	V
Gate to Source Leakage	$V_{GS} = \pm 15\text{ V}, T_J = 25^\circ\text{C}$	I_{GSS}	—	100	±200	nA
Zero Gate Voltage Drain Current	$V_{DS} = 200\text{ V}, V_{GS} = 0\text{ V}, T_J = 25^\circ\text{C}$	I_{DSS}	—	1	25	μA
	$V_{DS} = 200\text{ V}, V_{GS} = 0\text{ V}, T_J = 125^\circ\text{C}$		—	10	300	μA
Transconductance	$V_{DS} = 10\text{ V}, I_D = 60\text{ A}$	g_{fs}	85	100	-	S
Total Gate Charge	$V_{GS} = 10\text{ V}$	Q_g	—	800	950	nC
Gate to Source Charge	$V_{DS} = 100\text{ V}$	Q_{gs}	—	300	450	
Gate to Drain Charge	$I_D = 60\text{ A}$	Q_{gd}	—	120	250	
Turn on Delay Time	$V_{GS} = 10\text{ V}$	$t_{d(on)}$	—	200	350	nsec
Rise Time	$V_{DS} = 100\text{ V}$	t_r	—	100	200	
Turn off Delay Time	$I_D = 60\text{ A}$	$t_{d(off)}$	—	320	500	
Fall Time	$R_G = 1\text{ }\Omega, pw = 3\text{ }\mu\text{s}$	t_f	—	80	140	
Diode Forward Voltage	$I_F = 100\text{ A}, V_{GS} = 0\text{ V}$	V_{SD}	—	1.0	1.4	V
Diode Reverse Recovery Time	$I_F = 60\text{ A}, di/dt = 100\text{ A}/\mu\text{sec}$	t_{rr1}	—	390	—	nsec
		$I_{RM(rec)1}$	—	28	—	A
Peak Reverse Recovery Current	$I_F = 10\text{ A}, di/dt = 100\text{ A}/\mu\text{sec}$	Q_{rr1}	—	5.5	—	μC
		t_{rr2}	—	230	300	nsec
Reverse Recovery Charge	$I_F = 10\text{ A}, di/dt = 100\text{ A}/\mu\text{sec}$	$I_{RM(rec)2}$	—	17.5	—	A
		Q_{rr2}	—	2	3	μC
Safe Operating Area	$V_{DS} = 10\text{ V}, t = 1\text{ s}, T_J = 25^\circ\text{C}$	SOA1	75	-	-	A
	$V_{DS} = 100\text{ V}, t = 1\text{ s}, T_J = 25^\circ\text{C}$	SOA2	3	-	-	
Input Capacitance	$V_{GS} = 0\text{ V}$	C_{iss}	—	74,500	—	pF
Output Capacitance	$V_{DS} = 25\text{ V}$	C_{oss}	—	2650	—	
Reverse Transfer Capacitance	$f = 1\text{ MHz}$	C_{rss}	—	1000	—	

NOTES:

* Pulse Test: Pulse Width = 300μsec, Duty Cycle = 2%.

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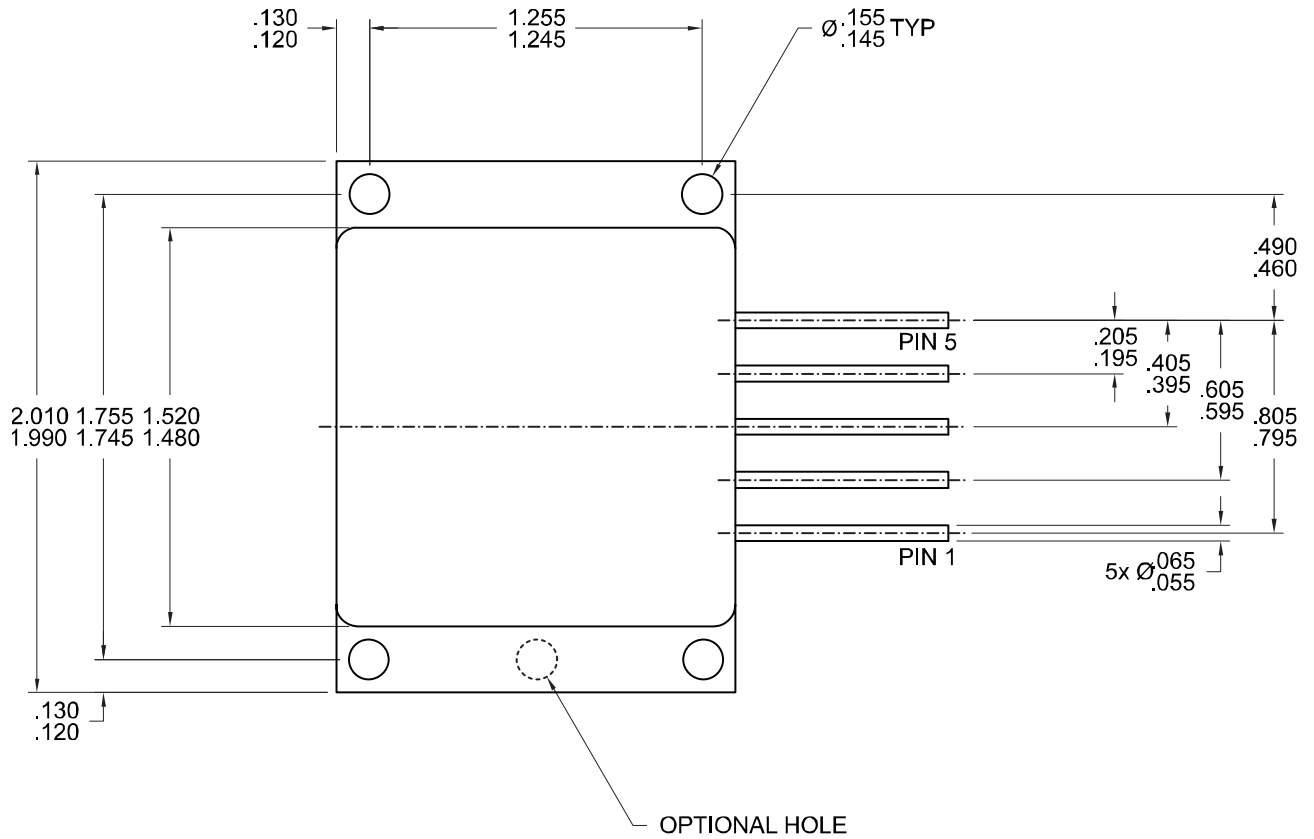


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SFF110P20FP5

CASE OUTLINE: 5 Pin Flat Pack (FP5)



Pin Assignment (Standard)

Drain	Source	Gate
Pin 1 & 2	Pin 3 & 4	Pin 5

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