Solid State Devices, Inc.
14701 Firestone Blvd * La Mirada, CA 90638
Phone: (562) 404-4474 * Fax: (562) 404-1773
ssdi@ssdi-power.com * www.ssdi-power.com

SFF120P20FP5
SFF120P20E

DESIGNER'S DATA SHEET

Part Number / Ordering Information 1/

SFF120P20 __ __ __

Screening 2/
__ = Not Screened
TX = TX Level
TXV = TXV Level
S = S Level

Lead Bend Options
__ = Straight Leads
DB = Down Bend
UB = Up Bend

Package
FP5 = 5 Pin Flat Pack
E = Milpack III

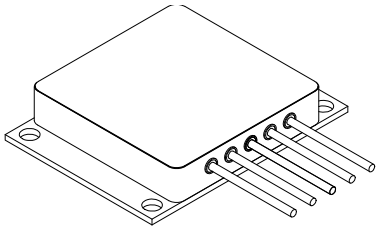
120 AMP
Avalanche Rated, Enhancement Mode
P-Channel MOSFET
200 Volts, 35 mΩ

Features:
- PolarMOS Technology
- Lowest ON-resistance in the Industry
- Avalanche Rated
- Hermetically Sealed Power Package
- Low Total Gate Charge
- Fast Switching
- TX, TXV, S-Level Screening Available 2/
- Improved ($R_{DS(ON)}$ Q_G) Figure of Merit

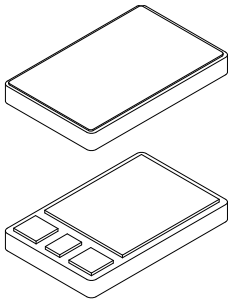
Maximum Ratings		Symbol	Value	Unit
Drain – Source Voltage		V_{DSS}	200	V
Gate – Source Voltage	Continuous Transient	V_{GS}	±20 ±30	V
Max. Continuous Drain Current (package limited)	@ T_C = 25°C	I_D	120	A
Source Current (Tj limited)	@ T_C = 25°C @ T_C = 125°C	I_S	135 40	A
Avalanche Energy		E_{AS}	7	J
Total Power Dissipation	@ T_C = 25°C	P_D	830	W
Operating & Storage Temperature		T_{OP} & T_{STG}	-55 to +150	°C
Maximum Thermal Resistance	Junction to Case	$R_{\theta JC}$	0.2	°C/W

NOTES:
1/ For ordering information, price, and availability - contact factory.
2/ Screening based on MIL-PRF-19500. Screening flows available on request.
3/ Unless otherwise specified, all electrical characteristics @ 25°C.

5 Pin Flat Pack (FP5)



Milpack III (E)



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Electrical Characteristics[3/]		Symbol	Min	Typ	Max	Unit
Drain to Source Breakdown Voltage	V_{GS} = 0 V, I_D = 0.25 mA	BV_{DSS}	200	230	—	**V**
Drain to Source On State Resistance	V_{GS} = 10 V, I_D = 75 A, T_J = 25°C V_{GS} = 10 V, I_D = 75 A, T_J = 125°C V_{GS} = 10 V, I_D = 120 A, T_J = 25°C	$R_{DS(on)}$	— — —	25 45 25	35 — —	**mΩ**
Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA, T_J = 25°C V_{DS} = V_{GS}, I_D = 250 µA, T_J = 125°C V_{DS} = V_{GS}, I_D = 250 µA, T_J = -55°C	$V_{GS(th)}$	2.0 — —	3.3 2.3 3.8	4.0 — 5.0	**V**
Gate to Source Leakage	V_{GS} = ±20 V, T_J = 25°C	I_{GSS}	—	20	±250	**nA**
Zero Gate Voltage Drain Current	V_{DS} = 200 V, V_{GS} = 0 V, T_J = 25°C V_{DS} = 200 V, V_{GS} = 0 V, T_J = 125°C	I_{DSS}	— —	1 6	50 500	**µA** **µA**
Transconductance	V_{DS} = 10 V, I_D = 75 A	g_{fs}	20	90	—	**S**
Total Gate Charge **Gate to Source Charge** **Gate to Drain Charge**	V_{GS} = 10 V V_{DS} = 100 V I_D = 75 A	Q_g Q_{gs} Q_{gd}	— — —	260 90 100	— — —	**nC**
Turn on Delay Time **Rise Time** **Turn off Delay Time** **Fall Time**	V_{GS} = 10 V V_{DS} = 100 V I_D = 75 A	$t_{d(on)}$ t_r $t_{d(off)}$ t_f	— — — —	55 70 100 55	— — — —	**nsec**
Diode Forward Voltage	I_F = 75 A, V_{GS} = 0 V	V_{SD}	—	2.2	3.0	**V**
Diode Reverse Recovery Time **Peak Reverse Recovery Current** **Reverse Recovery Charge**	I_F = 10 A, di/dt = 100 A/µsec	t_{rr} $I_{RM(rec)}$ Q_{rr}	— — —	250 22 7.5	— — —	**nsec** **A** **µC**
Input Capacitance **Output Capacitance** **Reverse Transfer Capacitance**	V_{GS} = 0 V V_{DS} = 25 V f = 1 MHz	C_{iss} C_{oss} C_{rss}	— — —	16,500 3100 400	— — —	**pF**

NOTES:

*Pulsed per MIL-STD-750.
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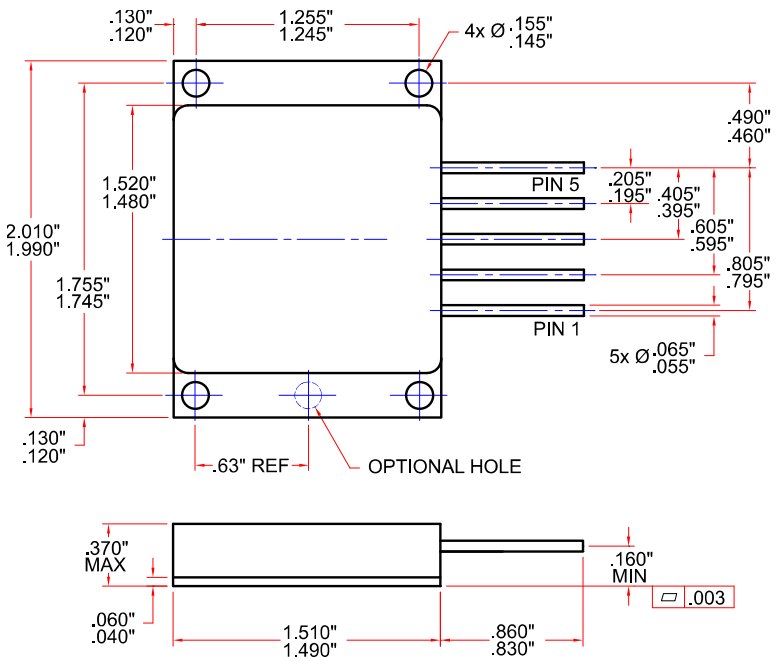
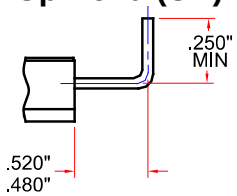
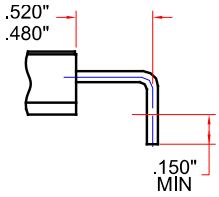
CASE OUTLINE: 5 Pin Flat Pack (FP5)



Up Bend (UB)

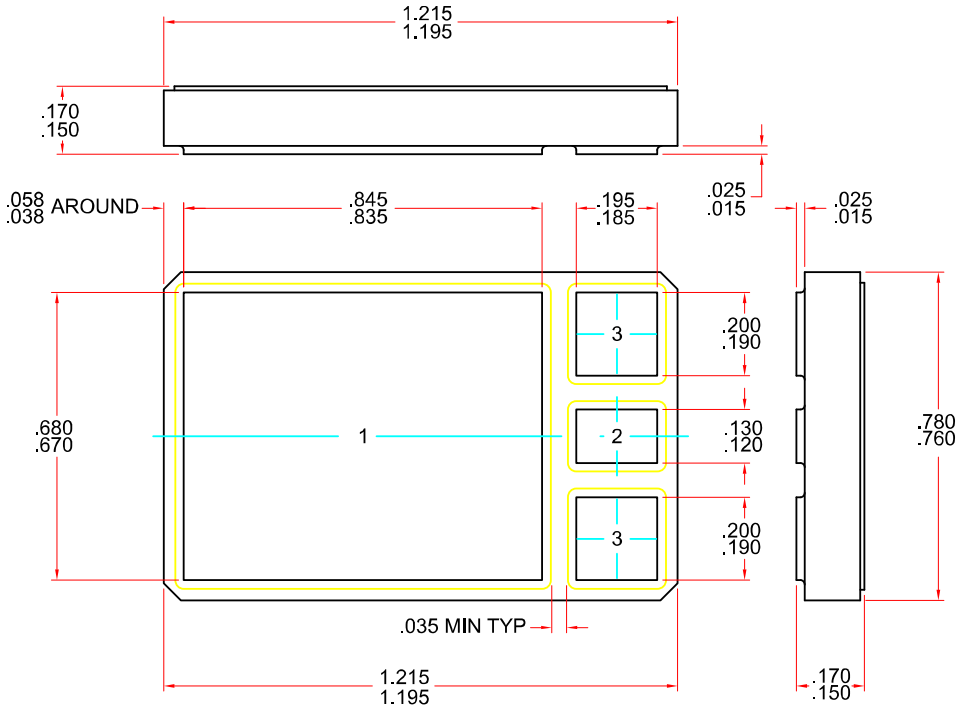


Down Bend (DB)



Pin Assignment (Standard)		
Drain	**Source**	**Gate**
Pin 1 & 2	**Pin 3 & 4**	**Pin 5**

CASE OUTLINE: Milpack III (E)



Pin Assignment (Standard)		
Drain	**Source**	**Gate**
Pin 1	**Pin 3**	**Pin 2**