



Solid State Devices, Inc.

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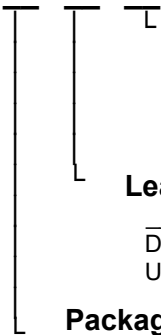
SFF28P20 Series

28 AMP , 200 Volts, 130 mΩ Avalanche Rated P-Channel TrenchFET

DESIGNER'S DATA SHEET

Part Number / Ordering Information ^{1/}

SFF28P20



Screening ^{2/}

 = Not Screened
TX = TX Level
TXV = TXV Level
S = S Level

Lead Option ^{3/}

 = Straight Leads
DB = Down Bend
UB = Up Bend

Package ^{3/ 4/}

M = TO-254
Z = TO-254Z

Features:

- TrenchMOS Technology
- Lowest ON-Resistance in the Industry
- Avalanche Rated
- Hermetically Sealed, Isolated Package
- Low Total Gate Charge
- Fast Switching
- TX, TXV, S-Level Screening Available
- Improved ($R_{DS(ON)}$ Q_G) Figure of Merit

Maximum Ratings ^{5/}	Symbol	Value	Units
Drain - Source Voltage	V_{DSS}	200	V
Gate - Source Voltage	V_{GS}	± 15 ± 25	V
Continuous Drain Current (T_{OP} limited) @ $T_C = 25^\circ C$	I_{D1}	28	A
Pulsed Drain Current (P_{width} / T_{OP} limited) @ $T_C = 25^\circ C$	I_{D3}	38	A
Single and Repetitive Avalanche Energy	E_{AS}	1000	mJ
Total Power Dissipation @ $T_C = 25^\circ C$	P_D	100	W
Operating & Storage Temperature	T_{OP} & T_{STG}	-55 to +150	$^\circ C$
Maximum Thermal Resistance (Junction to Case)	$R_{\theta JC}$	1.2	$^\circ C/W$

NOTES: *Pulse Test: Pulse Width = 300μsec, Duty Cycle = 2%.

1/ For ordering information, price, and availability - contact factory.

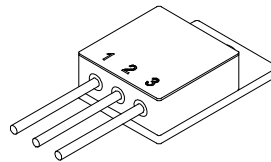
2/ Screening based on MIL-PRF-19500. Screening flows available on request.

3/ For lead bending options / pinout configurations - contact factory.

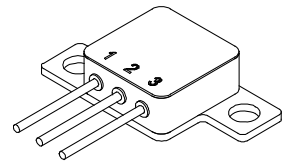
4/ Maximum current limited by package configuration

5/ Unless otherwise specified, all electrical characteristics @25°C.

TO-254 (M)



TO-254Z (Z)



NOTE: All specifications are subject to change without notification.
SCD's for these devices should be reviewed by SSDI prior to release.

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Electrical Characteristics ^{5/}		Symbol	Min	Typ	Max	Units
Drain to Source Breakdown Voltage	$V_{GS} = 0V, I_D = 0.25 \text{ mA}$	BV_{DSS}	200	1030	—	V
Drain to Source On State Resistance	$V_{GS} = 10V, I_D = 16A, T_j = 25^\circ C$ $V_{GS} = 10V, I_D = 16A, T_j = 125^\circ C$	$R_{DS(on)}$	—	75 140	130 —	m Ω
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 0.25 \text{ mA}, T_j = 25^\circ C$ $V_{DS} = V_{GS}, I_D = 0.25 \text{ mA}, T_j = 125^\circ C$ $V_{DS} = V_{GS}, I_D = 0.25 \text{ mA}, T_j = -55^\circ C$	$V_{GS(th)}$	2.0 1.0 —	3.0 2.1 3.5	4.0 — 5.0	V
Gate to Source Leakage	$V_{GS} = \pm 15V, T_j = 25^\circ C$ $V_{GS} = \pm 15V, T_j = 125^\circ C$	I_{GSS}	— —	10 10	± 200 —	nA
Zero Gate Voltage Drain Current	$V_{DS} = 200V, V_{GS} = 0V, T_j = 25^\circ C$ $V_{DS} = 200V, V_{GS} = 0V, T_j = 125^\circ C$	I_{DSS}	— —	0.5 6	25 200	μA μA
Transconductance	$V_{DS} = 10 \text{ V}, I_D = 16 \text{ A}$	g_{fs}	18	100	-	S
Total Gate Charge	$V_{GS} = 10V$	Q_g	—	215	350	nC
Gate to Source Charge	$V_{DS} = 100V$	Q_{gs}	—	75	125	
Gate to Drain Charge	$I_D = 16A$	Q_{gd}	—	35	70	
Turn on Delay Time	$V_{GS} = 10V$	$t_{d(on)}$	—	35	—	nsec
Rise Time	$V_{DS} = 100V$	t_r	—	17	—	
Turn off Delay Time	$I_D = 16A$	$t_{d(off)}$	—	160	—	
Fall Time		t_f	—	35	—	
Diode Forward Voltage	$I_F = 32A, V_{GS} = 0V$	V_{SD}	—	0.9	1.3	V
Diode Reverse Recovery Time	$I_F = 10A, di/dt = 100A/\mu sec$	t_{rr}	—	170	200	nsec
Reverse Recovery Charge	$I_F = 10A, di/dt = 100A/\mu sec$ $I_F = 10A, di/dt = 100A/\mu sec$	I_{rm} Q_{rr}	— —	13 1.1	17.5 —	A μC
Input Capacitance	$V_{GS} = 0V$	C_{iss}	—	16,000	—	pF
Output Capacitance	$V_{DS} = 50V$	C_{oss}	—	600	—	
Reverse Transfer Capacitance	$f = 1 \text{ MHz}$	C_{rss}	—	415	—	

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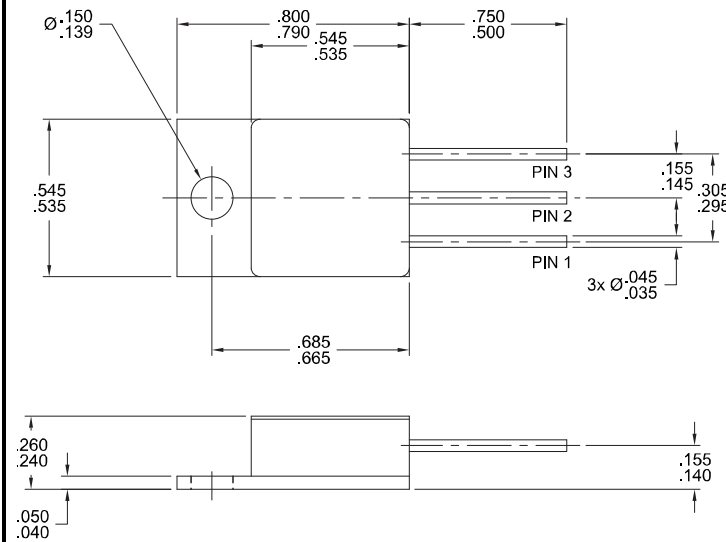


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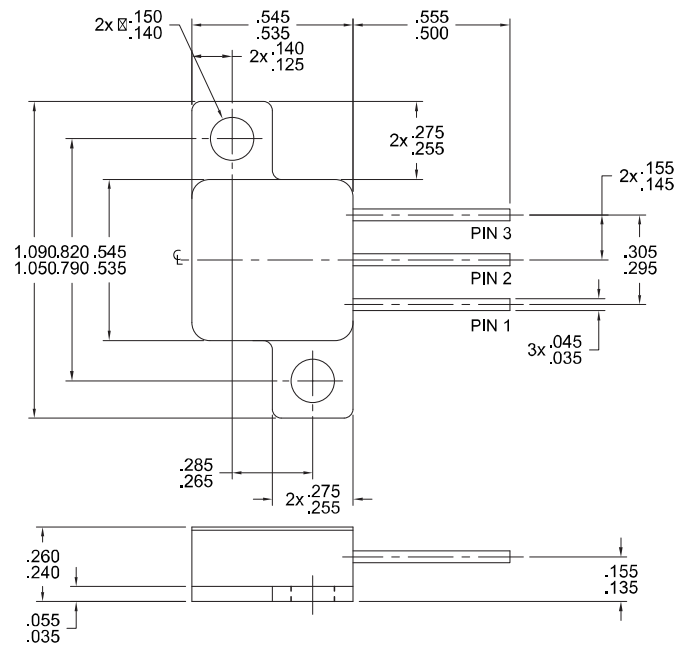
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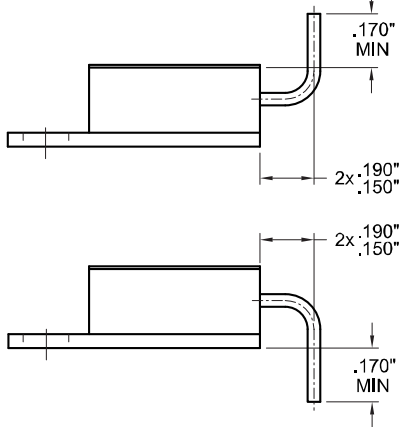
TO-254 (M)



TO-254Z (Z)



Lead Bend Options for TO-254 (M) and TO-254Z (Z)



PIN ASSIGNMENT (Standard)

Package	Drain	Source	Gate
TO-254 (M)	Pin 1	Pin 2	Pin 3
TO-254Z (Z)	Pin 1	Pin 2	Pin 3

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