

**Solid State Devices, Inc.**

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Designer's Data Sheet**Part Number/Ordering Information^{1/}****SGF48N10****Screening^{2/}**

___ = Not Screened
 TX = TX Level
 TXV = TXV Level
 S = S Level

**Lead Bend Options
(TO-254 only)**

___ = Straight Leads
 UB = Up Bend
 DB = Down Bend

Package

M = TO-254
 S1 = SMD1

SGF48N10M

SGF48N10S1

48 AMP
GaN POWER FET
Enhancement Mode
100 VOLTS, 8 – 10 mΩ**FEATURES:**

- 4th Generation Gallium Nitride Technology
- Exceptionally Low $R_{DS(ON)}$
- Low Q_G Simplifies Gate Drive Circuit
- Very Fast Switching for High-Freq. Applications
- Low Thermal Resistance
- Hermetically Sealed Package
- Available in Hermetically Sealed, Chip-Scale Package (SMG.3-1)
- TX, TXV, and S-Level Screening Available^{2/}

APPLICATIONS:

- High Efficiency DC-DC / PoL Converters
- Motor Controller
- Robotics/Automation
- Military and Aerospace

BENEFITS:

- GaN Transistor offers superior advantages over Si based MOSFET: zero Q_{RR} , low gate charge, low $R_{DS(ON)}$, fast switching speed and low temperature coefficient
- Benefits circuit designer through higher efficiency, lower cross-over losses and On-state losses
- Eliminates the need to add free-wheeling diode

Maximum Ratings ^{3/}	Symbol	Value	Units
Continuous Drain - Source Voltage	V_{DSS}	100	V
Gate – Source Voltage	V_{GS}	+6 -4	V
Continuous Drain Current	I_{D1}	48	A
Pulsed Drain Current T_{op} / P_{width} limited	I_{D2}	340	A
Total Power Dissipation	P_D	25	W
Operating & Storage Temperature	T_{OP} & T_{STG}	-55 to +150	°C
Thermal Resistance Junction to Case	$R_{\theta JC}$	5	°C/W

NOTES:

- 1/ For ordering information, price, operating curves, and availability- contact factory.
 2/ Screening based on MIL-PRF-19500. Screening flows available on request.
 3/ Unless otherwise specified, all electrical characteristics @ 25°C.
 4/ Pulse Test, $P_w = 300 \mu s$, D.C. = 2%.
 5/ Attach device with low temperature solder such as Sn63 with peak reflow temperature of 215°C and maximum dwell time of 30 sec.

SMD1 (S1)**TO-254 (M)**

NOTE: All specifications are subject to change without notification.
 SCD's for these devices should be reviewed by SSDI prior to release.

DATA SHEET #: FT0070D**DOCX**



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SGF48N10M SGF48N10S1

Electrical Characteristics ^{3/}	Symbol	Min	Typ	Max	Units
Drain to Source Breakdown Voltage $V_{GS} = 0\text{ V}, I_D = 0.8\text{ mA}$	BV_{DSS}	100	-	-	V
Gate to Source Leakage $V_{GS} = +5\text{ V}$ $V_{GS} = -4\text{ V}$	I_{GSS}	- -	1 0.1	9 0.6	mA
Zero Gate Voltage Drain Current $V_{DS} = 80\text{ V}, V_{GS} = 0\text{ V}, T_J = 25^\circ\text{C}$	I_{DSS}	-	0.1	0.6	mA
Gate Threshold Voltage $V_{DS} = V_{GS}, I_D = 11\text{ mA}, T_J = 25^\circ\text{C}$	$V_{GS(th)}$	0.8	1.4	2.5	V
Drain to Source On State Resistance^{4/} $V_{GS} = 5\text{ V}, I_D = 30\text{ A}, T_J = 25^\circ\text{C}$	$R_{DS(on)}$	- -	- -	8 10	mΩ
Source to Drain Forward Voltage^{4/} $I_F = 0.5\text{ A}, V_{GS} = 0\text{ V}$	V_{SD}	-	1.8	-	V
Total Gate Charge $V_{GS} = 5\text{ V}, V_{DS} = 50\text{ V}, I_D = 30\text{ A}$	Q_G	-	12	15	nC
Gate to Source Charge Gate to Drain Charge Gate Threshold Charge	Q_{GS} Q_{GD} Q_{GTH}	- - -	3.1 2 2.3	10 4 4.6	nC
Input Capacitance Output Capacitance Reverse Transfer Capacitance	C_{ISS} C_{OSS} C_{RSS}	- - -	1270 800 14	1530 1200 -	pF
Output Charge $V_{GS} = 0\text{ V}, V_{DS} = 50\text{ V}$	Q_{OSS}	-	66	100	nC
Source to Drain Recovery Charge	Q_{RR}	-	0	-	μC
Gate Resistance	R_G	-	0.4	-	Ω

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^{3/} Unless otherwise specified, all electrical characteristics @ 25°C.

^{4/} Pulse Test, $P_W = 300\text{ μs}$, D.C. = 2%.

^{5/} Attach device with low temperature solder such as Sn63 with peak reflow temperature of 215°C and maximum dwell time of 30 sec.

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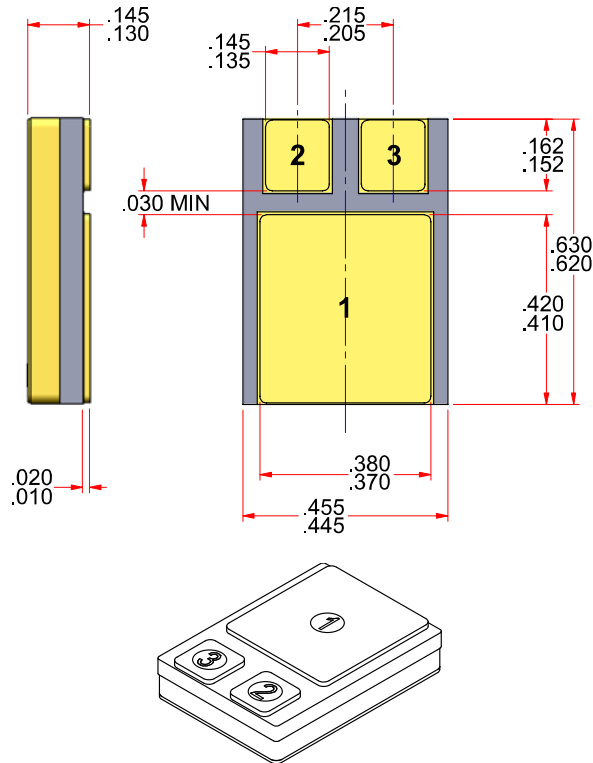
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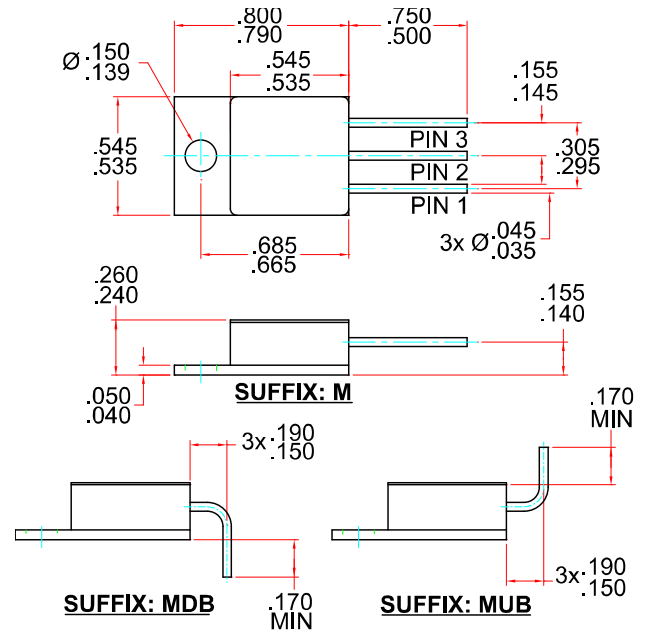
SGF48N10M SGF48N10S1

Package Outlines:

SMD1 (S1)



TO-254 (M)



AVAILABLE PART NUMBERS:

SMD1: SGF48N10S1

TO-254: SGF48N10M, SGF48N10MDB, SGF48N10MUB

Dimensions in inches

PIN ASSIGNMENT

	SMD1	TO-254
Source	1	2
Drain	3	1
Gate	2	3
Substrate	*	*

* Substrate internally tied to Source