Solid State Devices, Inc.
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SGF48N20M and SGF48N20S1

40 AMP
GaN POWER FET
Enhancement Mode
200 VOLTS, 14 – 16 mΩ

Designer's Data Sheet

Part Number/Ordering Information[1/]

SGF48N20 ___ ___ ___

- **Screening[2/]**
  - __ = Not Screened
  - TX = TX Level
  - TXV = TXV Level
  - S = S Level
- **Lead Bend Options**
  (TO-254 only)
  - __ = Straight Leads
  - UB = Up Bend
  - DB = Down Bend
- **Package**
  - M = TO-254
  - S1= SMD1

FEATURES:
- 4th Generation Gallium Nitride Technology
- Exceptionally Low $R_{DS(ON)}$
- Low Q_G Simplifies Gate Drive Circuit
- Very Fast Switching for High-Freq. Applications
- Low Thermal Resistance
- TX, TXV, and S-Level Screening Available[2/]

APPLICATIONS:
- High Efficiency DC-DC/PoL Converters
- Motor Controller
- Robotics/Automation
- Military and Aerospace

BENEFITS:
- GaN Transistor offers superior advantages over Si based MOSFET: Zero Q_{RR}, low gate charge, low $R_{DS(ON)}$, fast switching speed and low temperature coefficient
- Benefits circuit designer through higher efficiency, lower cross-over losses and On-state losses
- Eliminates the need to add free-wheeling diode

Maximum Ratings[3/]	Symbol	Value	Units
Continuous Drain - Source Voltage	V_{DSS}	200	V
Gate – Source Voltage	V_{GS}	+6 -4	V
Continuous Drain Current	I_{D1}	40	A
Pulsed Drain Current (T_{op} / P_{width} limited)	I_{D2}	200	A
Total Power Dissipation	P_D	25	W
Operating & Storage Temperature	T_{OP} & T_{STG}	-55 to +150	°C
Thermal Resistance (Junction to Case)	$R_{\theta JC}$	5	°C/W

NOTES:
1/ For ordering information, price, operating curves, and availability- contact factory.
2/ Screening based on MIL-PRF-19500. Screening flows available on request.
3/ Unless otherwise specified, all electrical characteristics @ 25°C.
4/ Pulse Test, P_W = 300 µs, D.C. = 2%.
5/ Attach device with low temperature solder such as Sn63 with peak reflow temperature of 215°C and maximum dwell time of 30 sec.

SMD1

TO-254

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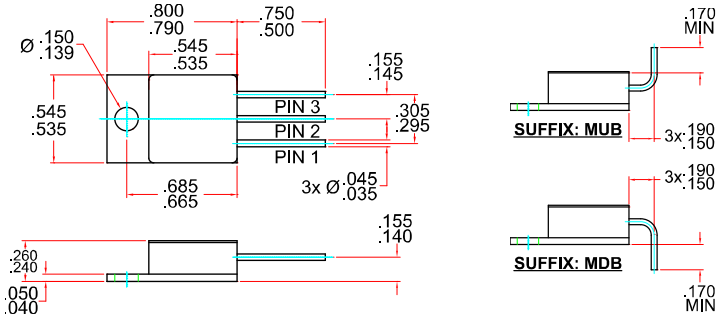
Electrical Characteristics[3]		Symbol	Min	Typ	Max	Units
Drain to Source Breakdown Voltage	V_{GS} = 0 V, I_D = 0.6 mA	BV_{DSS}	200	-	-	V
Gate to Source Leakage	V_{GS} = +5 V V_{GS} = -4 V	I_{GSS}	- -	1 0.1	7 0.4	mA
Zero Gate Voltage Drain Current	V_{DS} = 160 V, V_{GS} = 0 V	I_{DSS}	-	0.1	0.4	mA
Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 7 mA	$V_{GS(TH)}$	0.8	1.4	2.5	V
Drain to Source On State Resistance[4] V_{GS} = 5 V, I_D = 20 A	SMD1 TO-254	$R_{DS(ON)}$	- -	11 13	14 16	mΩ
Source to Drain Forward Voltage[4]	I_F = 0.5 A, V_{GS} = 0 V	V_{SD}	-	1.8	-	V
Total Gate Charge	V_{GS} = 5 V, V_{DS} = 100 V, I_D = 20 A	Q_G	-	9	11	nC
Gate to Source Charge Gate to Drain Charge Gate Threshold Charge	V_{DS} = 100 V I_D = 20 A	Q_{GS} Q_{GD} Q_{GTH}	- - -	3 1.8 2.2	- - -	nC
Input Capacitance Output Capacitance Reverse Transfer Capacitance	V_{GS} = 0 V V_{DS} = 100 V f = 1 MHz	C_{ISS} C_{OSS} C_{RSS}	- - -	950 450 2.3	1140 680 -	pF
Output Charge	V_{GS} = 0 V, V_{DS} = 100 V	Q_{OSS}	-	75	113	nC
Source to Drain Recovery Charge		Q_{RR}	-	0	-	µC
Gate Resistance		R_G	-	0.5	-	Ω

TO-254 (M)

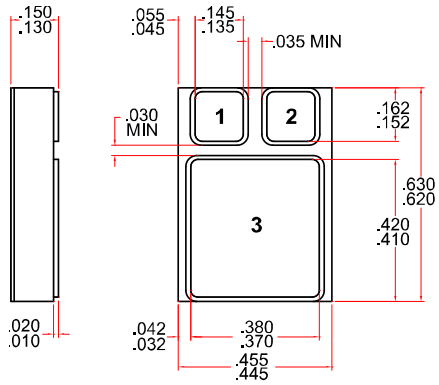


PIN ASSIGNMENT

	SMD1	TO-254
Source	3	2
Drain	2	1
Gate	1	3
Substrate	*	*

*Substrate internally tied to Source

SMD1 (S1)



AVAILABLE PART NUMBERS:
SMD1: SGF48N20S1
TO-254: SGF48N20M, SGF48N20MDB, SGF48N20MUB

Dimensions in inches

NOTE: All specifications are subject to change without notification.
SCD's for these devices should be reviewed by SSDI prior to release.

DATA SHEET #: FT0072A | **DOC**