



Solid State Devices, Inc.

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SFF80N20S1

**80 AMP , 200 Volts, 15 mΩ
Avalanche Rated
N-channel MOSFET**

DESIGNER'S DATA SHEET

Part Number / Ordering Information ^{1/}

SFF80N20

Screening ^{2/}

— = Not Screened
TX = TX Level
TXV = TXV Level
S = S Level

Package

S1 = SMD1

Features:

- Rugged poly-Si gate
- Lowest ON-resistance in the industry
- Avalanche rated
- Hermetically sealed surface mount package
- Low total gate charge
- Fast switching
- TX, TXV, S-Level screening available
- Improved ($R_{DS(ON)}$ Q_G) figure of merit

Maximum Ratings ^{3/}	Symbol	Value	Unit
Drain - Source Voltage	V_{DSS}	200	V
Gate – Source Voltage	V_{GS}	± 20 ± 30	V
Max. Continuous Drain Current (package limited)	I_{D1}	55	A
Max. Instantaneous Drain Current (Tj limited)	I_{D2} I_{D3}	80 48	A
Max. Avalanche Current	I_{AR}	80	A
Single and Repetitive Avalanche Energy @ $I_D = 80$ A	E_{AS}	500	mJ
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	150	W
Operating & Storage Temperature	T_{OP} & T_{STG}	-55 to +175	$^\circ\text{C}$
Maximum Thermal Resistance (Junction to Case)	$R_{\theta JC}$	0.55 (typ.0.4)	$^\circ\text{C/W}$

NOTES:

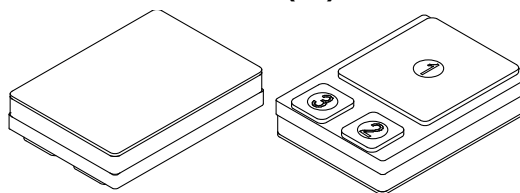
*Pulse Test: Pulse Width = 300 μsec , Duty Cycle = 2%.

^{1/} For ordering information, price, and availability - contact factory.

^{2/} Screening based on MIL-PRF-19500. Screening flows available on request.

^{3/} Unless otherwise specified, all electrical characteristics @ 25°C .

SMD1 (S1)



NOTE: All specifications are subject to change without notification.
SSD's for these devices should be reviewed by SSDI prior to release.

DATA SHEET #: FT0081B

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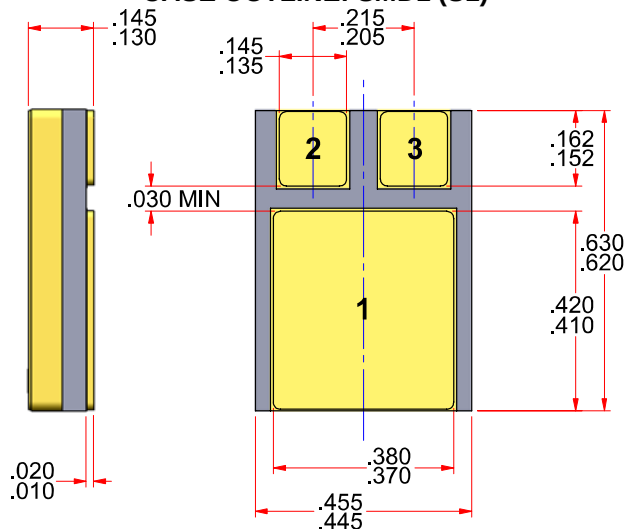
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Electrical Characteristics ^{3/}		Symbol	Min	Typ	Max	Unit
Drain to Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$	BV_{DSS}	200	215	—	V
Drain to Source On State Resistance	$V_{GS} = 10\text{ V}, I_D = 80\text{ A}, T_j = 25^\circ\text{C}$	$R_{DS(on)}$	—	15	20	mΩ
	$V_{GS} = 10\text{ V}, I_D = 80\text{ A}, T_j = 125^\circ\text{C}$		—	25	35	
	$V_{GS} = 10\text{ V}, I_D = 80\text{ A}, T_j = 175^\circ\text{C}$		—	35	—	
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = .25\text{ mA}, T_j = 25^\circ\text{C}$	$V_{GS(th)}$	2.0	3.0	4.0	V
	$V_{DS} = V_{GS}, I_D = .25\text{ mA}, T_j = 125^\circ\text{C}$		1.0	2.1	—	
	$V_{DS} = V_{GS}, I_D = .25\text{ mA}, T_j = -55^\circ\text{C}$		—	3.5	5	
Gate to Source Leakage	$V_{GS} = \pm 20\text{ V}, T_j = 25^\circ\text{C}$	I_{GSS}	—	10	±100	nA
	$V_{GS} = \pm 20\text{ V}, T_j = 125^\circ\text{C}$		—	30	—	
Zero Gate Voltage Drain Current	$V_{DS} = 200\text{ V}, V_{GS} = 0\text{ V}, T_j = 25^\circ\text{C}$	I_{DSS}	—	0.1	1	μA
	$V_{DS} = 200\text{ V}, V_{GS} = 0\text{ V}, T_j = 125^\circ\text{C}$		—	10	100	μA
	$V_{DS} = 200\text{ V}, V_{GS} = 0\text{ V}, T_j = 175^\circ\text{C}$		—	250	—	μA
Forward Transconductance	$V_{DS} = 2.50\text{ V}, I_D = 80\text{ A}, T_j = 25^\circ\text{C}$	g_{fs}	50	70	—	Mho
Total Gate Charge	$V_{GS} = 10\text{ V}$	Q_g	—	65	100	nC
Gate to Source Charge	$V_{DS} = 100\text{ V}$	Q_{gs}	—	24	35	
Gate to Drain Charge	$I_D = 44\text{ A}$	Q_{gd}	—	13	20	
Turn on Delay Time	$V_{GS} = 10\text{ V}$	$t_{d(on)}$	—	35	75	nsec
Rise Time	$V_{DS} = 100\text{ V}$	t_r	—	32	65	
Turn off Delay Time	$I_D = 44\text{ A}$	$t_{d(off)}$	—	65	125	
Fall Time	$R_G = 1.6\text{ }\Omega, p_w = 3\text{ }\mu\text{s}$	t_f	—	20	45	
Diode Forward Voltage	$I_F = 88\text{ A}, V_{GS} = 0\text{ V}$	V_{SD}	—	1.35	1.5	V
Diode Reverse Recovery Time	$I_F = 44\text{ A}, di/dt = 100\text{ A}/\mu\text{sec}$	t_{rr}	—	160	200	nsec
Reverse Recovery Charge		Q_{rr}	—	850	—	nC
Input Capacitance	$V_{GS} = 0\text{ V}$	C_{iss}	—	6200	—	pF
Output Capacitance	$V_{DS} = 100\text{ V}$	C_{oss}	—	400	—	
Reverse Transfer Capacitance	$f = 1\text{ MHz}$	C_{rss}	—	—	—	

CASE OUTLINE: SMD1 (S1)



PIN ASSIGNMENT (Standard)

Package	Drain	Source	Gate
SMD1	Pin 1	Pin 2	Pin 3

NOTES:

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