Solid State Devices, Inc.
14701 Firestone Blvd * La Mirada, CA 90638
Phone: (562) 404-4470 * Fax: (562) 404-1773
ssdi@ssdi-power.com * www.ssdi-power.com

SFF75P10S2

DESIGNER'S DATA SHEET

-75 AMP
P-Channel POWER MOSFET
-100 Volts
0.045 Ω

Part Number / Ordering Information 1/

SFF75P10

Screening2/
- __ = Not Screened
- TX = TX Level
- TXV = TXV Level
- S = S Level

Package
- S2 = SMD2

Features:
- Rugged Construction with Poly Silicon Gate
- Low RDS(on) and High Transconductance
- Excellent High Temperature Stability
- Very Fast Switching Speed
- Fast Recovery and Superior dv/dt Performance
- Increased Reverse Energy Capability
- Low Input and Transfer Capacitance for Easy Paralleling
- Hermetically Sealed
- TX, TXV, and Space Level Screening Available
- Replaces IRF9160 Types

Maximum Ratings3/		Symbol	Value	Unit
Drain – Source Voltage		V_{DS}	-100	V
Gate – Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C = 25°C T_C = 100°C	I_{D1} I_{D2}	-75 -38	A
Pulsed Drain Current (construction limited)	T_C = 25°C	I_{D3}	-90	A
Operating & Storage Temperature		T_{OP} & T_{STG}	-55 to +150	°C
Thermal Resistance, Junction to Case		$R_{\Theta JC}$	0.5 (typ 0.35)	°C/W
Total Device Power Dissipation	T_C = 25°C	P_D	250	W
Single Pulse Avalanche Energy		E_{AS}	500	mJ

NOTES:

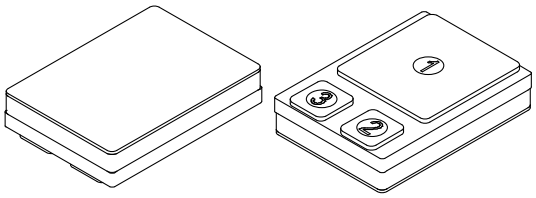
*Pulsed per MIL-STD-750.

1/ For ordering information, price, and availability - contact factory.

2/ Screening based on MIL-PRF-19500. Screening flows available on request.

3/ Unless otherwise specified, all electrical characteristics @ 25°C.

SMD2 (S2)



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Electrical Characteristics[3/]		Symbol	Min	Typ	Max	Unit
Drain to Source Breakdown Voltage (V_{GS} = 0 V, I_D = -1 mA)		BV_{DSS}	-100	-110	—	V
Drain to Source On State Resistance (V_{GS} = -12 V)	I_D = -30 A	$R_{DS(on)}$	—	30.5	45	mΩ
	I_D =-30 A, T_J =-55°C		—	18	—	
	I_D =-30 A, T_J =125°C		—	53	70	
	I_D = -60 A		—	32.5	—	
	I_D =-60 A, T_J =-55°C		—	20	—	
	I_D =-60 A, T_J =125°C		—	56	—	
	I_D = -90 A		—	35	45	
	I_D =-90 A, T_J =-55°C		—	20	—	
	I_D =-90 A, T_J =125°C		—	62	—	
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = -1.0 mA)		$V_{GS(th)}$	-2.0	-3.4	-4.0	V
Forward Transconductance (V_{DS} = -15 V)	I_D = -30 A	g_{fs}	—	25	—	S
	I_D = -60 A		25	37	—	
Zero Gate Voltage Drain Current (V_{DS} = -100 V, V_{GS} = 0 V)		I_{DSS}	—	-0.2	-10	μA
(V_{DS} = -100V, V_{GS} = 0 V, T_J = 125°C)			—	-1	-100	
Gate to Source Leakage Forward	V_{GS} = -20 A	I_{GSS}	—	-10	-100	nA
Gate to Source Leakage Reverse	V_{GS} = 20 A		—	10	100	
Total Gate Charge	I_D = -30 A	Q_g	—	165	250	nC
Gate to Source Charge	V_{DS} = -50 V	Q_{gs}	—	30	55	
Gate to Drain Charge	V_{GS} = -12 V	Q_{gd}	—	75	125	
Turn on Delay Time	V_{DD} = -50 V	$t_{(on)}$	—	45	65	nsec
Rise Time	I_D = -30 A	t_r	—	115	170	
Turn off Delay Time		$t_{d(off)}$	—	170	250	
Fall Time	V_{GS} = -12 V	t_f	—	115	150	
Diode Forward Voltage (V_{GS} = 0 V)	I_S = -60 A	V_{SD}	—	-1.00	-1.5	V
	I_S = -90 A		—	-1.10	—	
Diode Reverse Recovery Time	T_J = 25°C	t_{RR}	—	160	300	nsec
Reverse Recovery Charge	I_F = -10 A, dI/dt = 100 A/μsec	Q_{RR}	—	1.2	1.8	μC
Input Capacitance	V_{GS} = 0 V	C_{iss}	—	4000	—	pF
Output Capacitance	V_{DS} = -25 V	C_{oss}	—	1300	—	
Reverse Transfer Capacitance	f = 1 MHz	C_{rss}	—	690	—	

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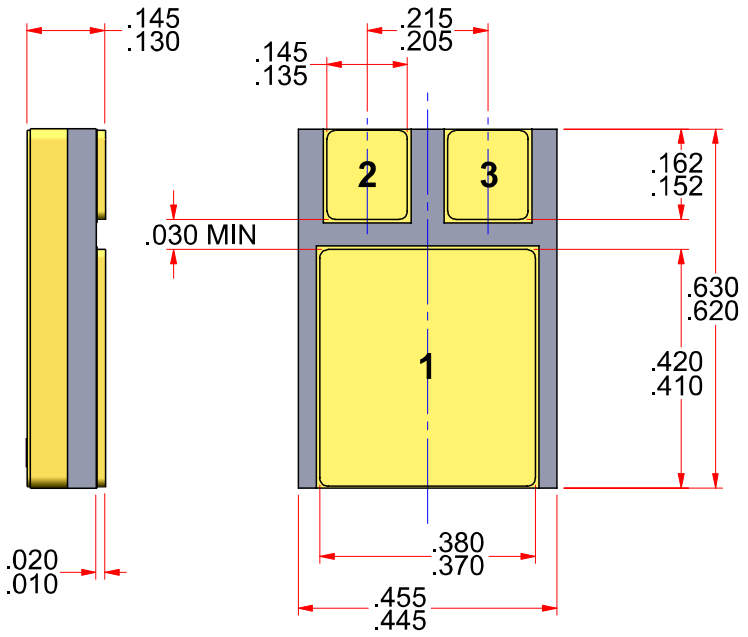
PACKAGE OUTLINE: SMD2 (S2)



Bottom View

Available Part Numbers:

SFF75P10S2

PIN ASSIGNMENT (Standard)			
Package	**Drain**	**Source**	**Gate**
SMD2 (S2)	Pin 1	Pin 2	Pin 3