



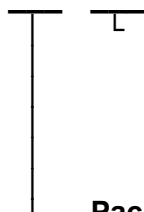
Solid State Devices, Inc.

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Phone: (562) 404-4474 * Fax: (562) 404-1773
ssdi@ssdi-power.com * www.ssdi-power.com

DESIGNER'S DATA SHEET

Part Number / Ordering Information ^{1/}

SFF225N10



Screening ^{2/}

— = Not Screened
TX = TX Level
TXV = TXV Level
S = S Level

Package ^{3/ 4/}

S2 = SMD2

SFF225N10S2

225 AMPpk, 100 VOLTS, 2.5 mΩ
High Operating Temperature
Avalanche Rated
N-Channel MOSFET

Features:

- Rugged Poly-Si Gate
- Lowest ON-Resistance in the Industry
- Extended Operating Temperature Range
- Avalanche Rated
- Hermetically Sealed, Isolated Package
- Low Total Gate Charge
- Fast Switching
- TX, TXV, S-Level Screening Available

Maximum Ratings	Symbol	Value	Unit
Drain – Source Voltage	V_{DS}	100	V
Gate – Source Voltage	V_{GS}	± 20 ± 30	V
Max. Continuous Drain Current (Package limited)	I_{D1}	110	A
Max. Instantaneous Drain Current (Tj limited)	I_{D2}	225	A
Max. Avalanche Current	I_{AR}	110	A
Single Avalanche Energy	E_{AS}	2000	mJ
Total Power Dissipation	P_D	250	W
Operating & Storage Temperature	T_{OP} & T_{STG}	-55 to +175	°C
Maximum Thermal Resistance (Junction to Case)	$R_{\theta JC}$	0.5 (typ.0.3)	°C/W

NOTES: *Pulsed per MIL-STD-750.

^{1/} For ordering information, price, and availability - contact factory.

^{2/} Screening based on MIL-PRF-19500. Screening flows available on request.

^{3/} For package outlines / lead bending options / pinout configurations - contact factory.

^{4/} Maximum current limited by package configuration.

^{5/} Unless otherwise specified, all electrical characteristics @25°C.

SMD2 (S2)



NOTE: All specifications are subject to change without notification.
SSD's for these devices should be reviewed by SSDI prior to release.

DATA SHEET #: FT0107A

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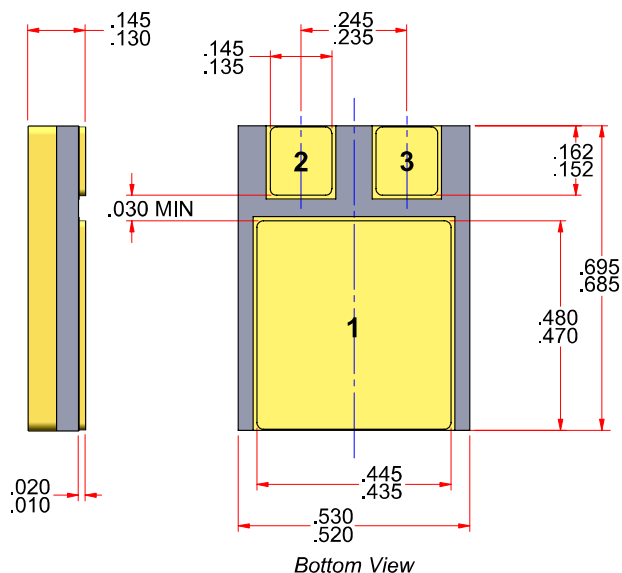
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SFF225N10S2

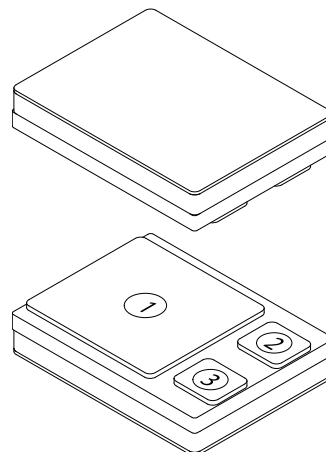
Electrical Characteristics ^{5/}		Symbol	Min	Typ	Max	Unit
Drain to Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	BV_{DSS}	100	110	—	V
Drain to Source On State Resistance	$V_{GS} = 10\text{ V}, I_D = 50\text{ A}, T_J = 25^\circ\text{C}$	$R_{DS(on)}$	—	1.75	—	m Ω
	$V_{GS} = 10\text{ V}, I_D = 100\text{ A}, T_J = 25^\circ\text{C}$		—	1.85	2.5	
	$V_{GS} = 10\text{ V}, I_D = 100\text{ A}, T_J = 125^\circ\text{C}$		—	2.55	3	
	$V_{GS} = 10\text{ V}, I_D = 100\text{ A}, T_J = -55^\circ\text{C}$		—	1.25	—	
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 5.0\text{ mA}, T_J = 25^\circ\text{C}$	$V_{GS(th)}$	2.0	3.0	4.0	V
	$V_{DS} = V_{GS}, I_D = 5.0\text{ mA}, T_J = 125^\circ\text{C}$		1.0	2.3	—	
	$V_{DS} = V_{GS}, I_D = 5.0\text{ mA}, T_J = -55^\circ\text{C}$		—	3.8	5.0	
Gate to Source Leakage	$V_{GS} = \pm 20\text{ V}, T_J = 25^\circ\text{C}$	I_{GSS}	—	20	± 200	nA
	$V_{GS} = \pm 20\text{ V}, T_J = 125^\circ\text{C}$		—	50	—	
Zero Gate Voltage Drain Current	$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}, T_J = 25^\circ\text{C}$	I_{DSS}	—	0.1	10	μA
	$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}, T_J = 125^\circ\text{C}$		—	25	200	
Forward Transconductance	$V_{DS} = 15\text{ V}, I_D = 70\text{ A}, T_J = 25^\circ\text{C}$	g_{fs}	30	75	—	Mho
Total Gate Charge	$V_{GS} = 12\text{ V}$	Q_g	—	320	450	nC
Gate to Source Charge	$V_{DS} = 35\text{ V}$	Q_{gs}	—	110	170	
Gate to Drain Charge	$I_D = 100\text{ A}$	Q_{gd}	—	65	100	
Turn on Delay Time	$V_{GS} = 11\text{ V}$	$t_{d(on)}$	—	125	200	nsec
Rise Time	$V_{DS} = 50\text{ V}$	t_r	—	90	130	
Turn off Delay Time	$I_D = 70\text{ A}$	$t_{d(off)}$	—	260	400	
Fall Time	$R_G = 2.35\text{ }\Omega, pw = 3\text{ }\mu\text{s}$	t_f	—	110	175	
Diode Forward Voltage	$I_F = 35\text{ A}, V_{GS} = 0\text{ V}$	V_{SD}	—	0.80	1.0	V
Diode Reverse Recovery Time	$I_F = 100\text{ A}, di/dt = 100\text{ A}/\mu\text{sec}$	t_{rr}	—	160	300	nsec
		Q_{rr}	—	700	—	nC
Input Capacitance	$V_{GS} = 0\text{ V}$	C_{iss}	—	20000	—	pF
Output Capacitance	$V_{DS} = 12\text{ V}$	C_{oss}	—	11000	—	
Reverse Transfer Capacitance	$f = 1\text{ MHz}$	C_{rss}	—	2500	—	

SMD2 (S2)



PIN ASSIGNMENT (Standard)

Package	Drain	Source	Gate
SMD2 (S2)	Pin 1	Pin 2	Pin 3



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