Solid State Devices, Inc.
14701 Firestone Blvd * La Mirada, Ca 90638
Phone: (562) 404-4474 * Fax: (562) 404-1773
ssdi@ssdi-power.com * www.ssdi-power.com

SFF225N10N/P

225 AMPpk , 100 Volts, 5.5 mΩ High Operating Temperature Avalanche Rated N-Channel MOSFET

DESIGNER'S DATA SHEET

Part Number / Ordering Information 1/

SFF225N10 __ __ __

Screening 2/
- __ = Not Screened
- TX = TX Level
- TXV = TXV Level
- S = S Level

Lead Bend Options
- __ = Straight Leads
- DB = Down Bend
- UB = Up Bend

Package
- N = TO-258
- P = TO-259

Features:
- Rugged Poly-Si Gate
- Lowest ON-Resistance in the Industry
- Extended Operating Temperature Range
- Avalanche Rated
- Hermetically Sealed, Isolated Package
- Low Total Gate Charge
- Fast Switching
- TX, TXV, S-Level Screening Available

Maximum Ratings		Symbol	Value	Unit
Drain – Source Voltage		V_{DSS}	100	V
Gate – Source Voltage	continuous transient	V_{GS}	±20 ±30	V
Max. Continuous Drain Current (package limited)	@ T_C = 25°C	I_{D1}	75	A
Max. Instantaneous Drain Current (Tj limited)	@ T_C = 25°C	I_{D2}	225	A
Max. Avalanche Current	@ L = 0.1 mH	I_{AR}	110	A
Single Avalanche Energy	@ L = 0.1 mH	E_{AS}	2000	mJ
Total Power Dissipation	@ T_C = 25°C	P_D	250	W
Operating & Storage Temperature		T_{OP} & T_{STG}	-55 to +175	°C
Maximum Thermal Resistance (Junction to Case)		$R_{\theta JC}$	0.55 (typ.0.4)	°C/W

Notes: *Pulsed per MIL-STD-750.

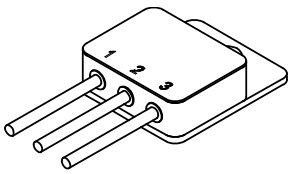
1/ For ordering information, price, and availability, contact factory.

2/ Screening based on MIL-PRF-19500. Screening flows available on request.

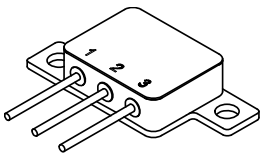
3/ Unless otherwise specified, all electrical characteristics @25ºC

4/ If High temp operation is desired (>175°C), consult factory for soldering consideration.

TO-258 (N)



TO-259 (P)



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Electrical Characteristics[5/]		Symbol	Min	Typ	Max	Unit
Drain to Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	BV_{DSS}	100	110	—	**V**
Drain to Source On State Resistance	V_{GS} = 10 V, I_D = 50 A, T_J = 25°C V_{GS} = 10 V, I_D = 100 A, T_J = 25°C V_{GS} = 10 V, I_D = 100 A, T_J =125°C V_{GS} = 10 V, I_D = 100 A, T_J =-55°C	$R_{DS(on)}$	— — — —	4.2 4.2 5.6 2.8	— 5.5 7 —	**mΩ**
Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 5.0 mA, T_J = 25°C V_{DS} = V_{GS}, I_D = 5.0 mA, T_J = 125°C V_{DS} = V_{GS}, I_D = 5.0 mA, T_J = -55°C	$V_{GS(th)}$	2.0 1.0 —	3.0 2.3 3.8	4.0 — 5.0	**V**
Gate to Source Leakage	V_{GS} = ±20 V, T_J = 25°C V_{GS} = ±20 V, T_J = 125°C	I_{GSS}	— —	20 50	±200 —	**nA**
Zero Gate Voltage Drain Current	V_{DS} = 100 V, V_{GS} = 0 V, T_J = 25°C V_{DS} = 100 V, V_{GS} = 0 V, T_J = 125°C	I_{DSS}	— —	0.1 25	10 200	**µA** **µA**
Forward Transconductance	V_{DS} = 15 V, I_D = 70 A, T_J = 25°C	g_{fs}	30	75	—	**Mho**
Total Gate Charge **Gate to Source Charge** **Gate to Drain Charge**	V_{GS} = 12 V V_{DS} = 35 V I_D = 100 A	Q_g Q_{gs} Q_{gd}	— — —	320 110 65	450 170 100	**nC**
Turn on Delay Time **Rise Time** **Turn off Delay Time** **Fall Time**	V_{GS} = 11 V V_{DS} = 50 V I_D = 70 A R_G = 2.35 Ω, pw = 3 µs	$t_{d(on)}$ t_r $t_{d(off)}$ t_f	— — — —	125 90 260 110	200 130 400 175	**nsec**
Diode Forward Voltage	I_F = 35 A, V_{GS} = 0 V	V_{SD}	—	0.80	1.0	**V**
Diode Reverse Recovery Time **Reverse Recovery Charge**	I_F = 100 A, di/dt = 100 A/µsec	t_{rr} Q_{rr}	— —	160 700	300 —	**nsec** **nC**
Input Capacitance **Output Capacitance** **Reverse Transfer Capacitance**	V_{GS} = 0 V V_{DS} = 12 V f = 1 MHz	C_{iss} C_{oss} C_{rss}	— — —	20000 11000 2500	— — —	**pF**

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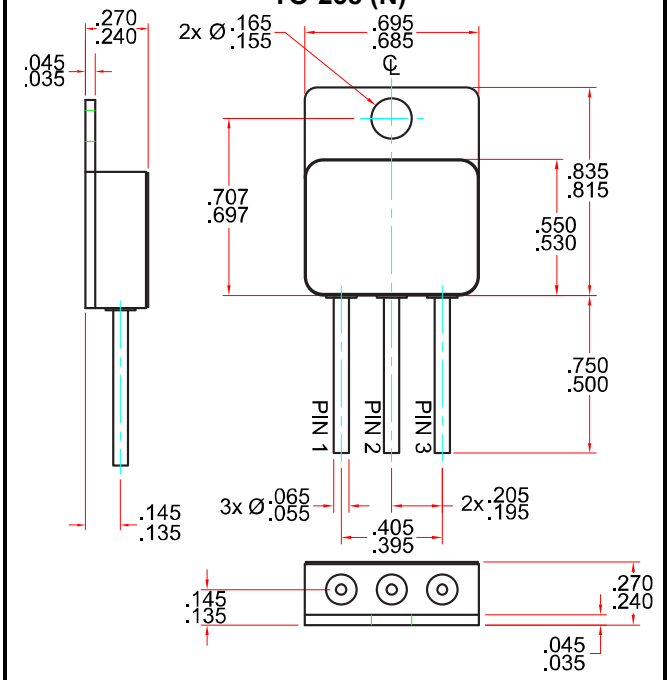
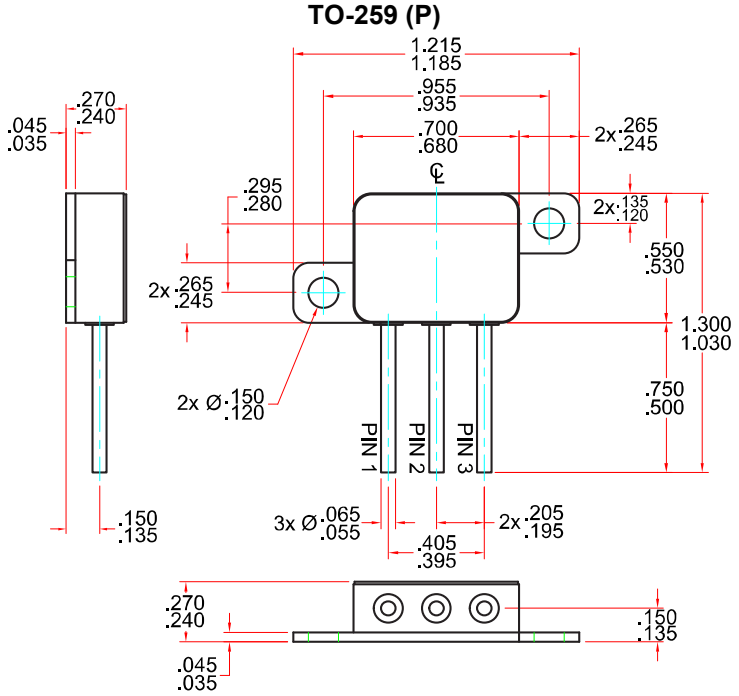
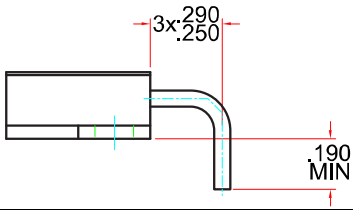
TO-258 (N)



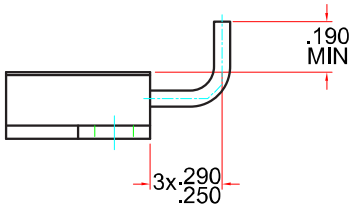
TO-259 (P)



Down Bend (DB)



Up Bend (UB)



PIN ASSIGNMENT (Standard)

Package	Drain	Source	Gate
TO-258 (N)	Pin 1	Pin 2	Pin 3
TO-259 (P)	Pin 1	Pin 2	Pin 3