



Solid State Devices, Inc.

14701 Firestone Blvd * La Mirada, Ca 90638
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DESIGNER'S DATA SHEET

Part Number / Ordering Information ^{1/}

SPH 24 100 FP

Screening ^{2/}
 — = Commercial
 H = Class H level
 K = Class K Level

Lead Bend Options
 — = Straight
 UB = Up Bend
 DB = Down Bend

Package ^{3/}
 FP = Flat pack – 12 Pin Package

Voltage
 100 = 1000 V

Current
 24 = 24 A

SPH24100FP

24 AMP , 1000 Volts, 0.18 Ω
Half-Bridge, N-Channel MOSFET
Hi-Rel POWER HYBRID

Features:

- Rugged poly-Si gate
- Lowest ON-resistance in the Industry
- Avalanche rated
- Hermetically Sealed, Isolated Package
- Low Total Gate Charge
- Fast Switching
- Improved ($R_{DS(ON)}$, Q_G) Figure of Merit
- Class H, K Screening Available ^{2/}
- Consult Factory for Special Requirements such as Built-in Zener Diode Protection, Gate Resistor, Anti-Parallel Diode for Faster Switching, etc.

Typical Applications:

- Airborne/Aerospace
- Motor Controls
- Inverters

Maximum Ratings (per side) ^{3/}	Symbol	Value	Units
Drain - Source Voltage	V_{DSS}	1000	V
Gate – Source Voltage	V_{GS}	$\begin{matrix} +20 \\ +30 \end{matrix}$	V
Continuous Drain Current (Lead $\leq 0.3"$, Top Limited)	I_{D1} I_{D2}	$\begin{matrix} 24 \\ 15 \end{matrix}$	A
Pulsed Drain Current (Pulse Width/Top Limited)	I_{D3}	75	A
Single and Repetitive Avalanche Energy	E_{AS} E_{AR}	$\begin{matrix} 1200 \\ 2 \end{matrix}$	mJ
Total Power Dissipation	P_D	250	W
Operating & Storage Temperature	T_{OP} & T_{STG}	-55 to +150	$^{\circ}C$
Thermal Resistance (Junction to Case)	$R_{\theta JC}$	0.5	$^{\circ}C/W$

NOTES:

*Pulse Test: Pulse Width = 300 μ sec, Duty Cycle = 2%.

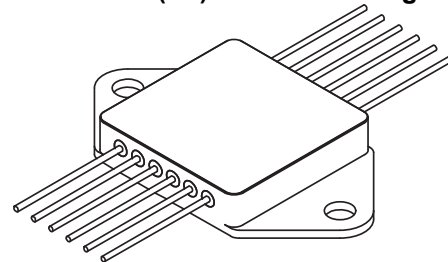
^{1/} For ordering information, price, and availability – contact factory.

^{2/} Screening based on MIL-PRF-38534. Screening flows available on request.

^{3/} Unless otherwise specified, all electrical characteristics @25 $^{\circ}C$.

^{4/} All Drain and Source Pins are utilized

Flat Pack (FP) – 12 Pin Package



NOTE: All specifications are subject to change without notification.
SCD's for these devices should be reviewed by SSDI prior to release.

DATA SHEET #: PH0002A

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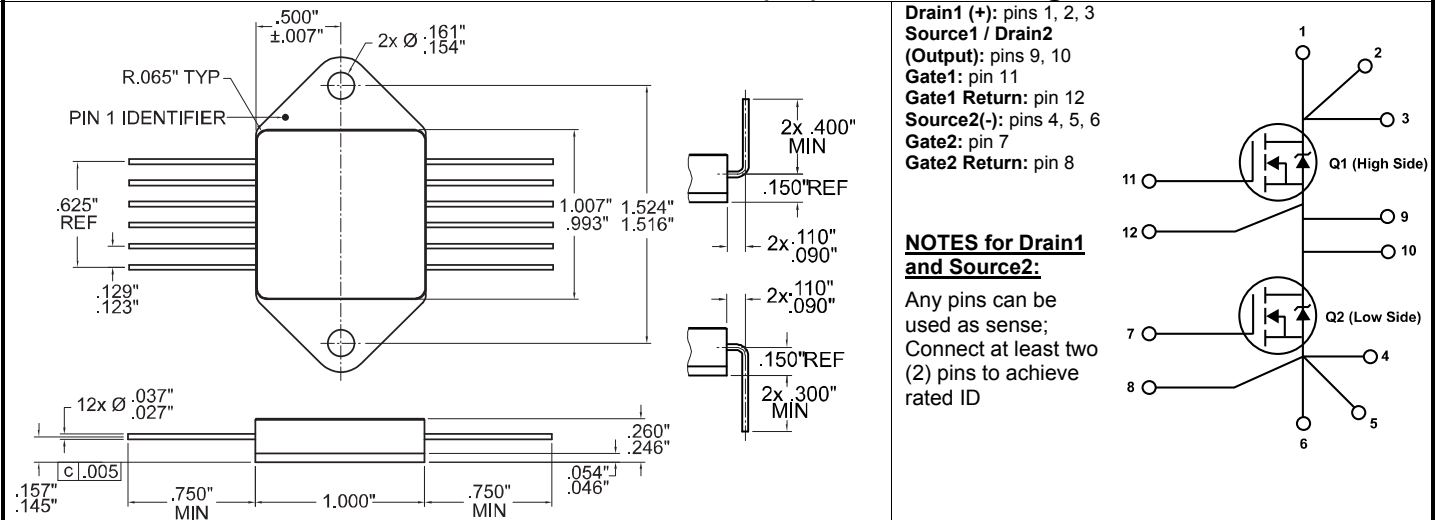
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SPH24100FP

Electrical Characteristics (per side) ^{3/}		Symbol	Min	Typ	Max	Units
Drain to Source Breakdown Voltage	$V_{GS} = 0V, I_D = 0.5 \text{ mA}$	BV_{DSS}	1000	1030	—	V
Drain to Source On State Resistance^{4/}	$V_{GS} = 10V, I_D = 20A, T_J = 25^\circ C$ $V_{GS} = 10V, I_D = 20A, T_J = 150^\circ C$	$R_{DS(on)}$	— —	168 428	180 —	mΩ
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 2 \text{ mA}, T_J = 25^\circ C$ $V_{DS} = V_{GS}, I_D = 2 \text{ mA}, T_J = 125^\circ C$ $V_{DS} = V_{GS}, I_D = 2 \text{ mA}, T_J = -55^\circ C$	$V_{GS(th)}$	2.5 1.5 —	3.0 2.0 4.0	3.5 — 4.5	V
Gate to Source Leakage	$V_{GS} = \pm 20V, T_J = 25^\circ C$ $V_{GS} = \pm 20V, T_J = 125^\circ C$	I_{GSS}	— —	1 10	± 200 —	nA
Zero Gate Voltage Drain Current	$V_{DS} = 900V, V_{GS} = 0V, T_J = 25^\circ C$ $V_{DS} = 900V, V_{GS} = 0V, T_J = 150^\circ C$	I_{DSS}	— —	0.02 10	5 300	μA μA
Total Gate Charge	$V_{GS} = 10V$	Q_g	—	200	300	nC
Gate to Source Charge	$V_{DS} = 150V$	Q_{gs}	—	25	50	nC
Gate to Drain Charge	$I_D = 20A$	Q_{gd}	—	80	150	nC
Turn on Delay Time	$V_{GS} = 10V$	$t_{d(on)}$	—	45	75	nsec
Rise Time	$V_{DS} = 150V$	t_r	—	20	35	
Turn off Delay Time	$I_D = 20A$	$t_{d(off)}$	—	150	250	
Fall Time		t_f	—	15	40	
Diode Forward Voltage^{4/}	$I_F = 20A, V_{GS} = 0V$	V_{SD}	—	0.95	1.15	V
Diode Reverse Recovery Time	$I_F = 10A, di/dt = 100A/\mu sec$	t_{rr1}	—	400	600	nsec
Reverse Recovery Charge	$I_F = 10A, di/dt = 100A/\mu sec$	I_{rm1}	—	27	—	A
	$I_F = 10A, di/dt = 100A/\mu sec$	Q_{rr1}	—	5.5	—	μC
Input Capacitance	$V_{GS} = 0V$	C_{iss}	—	5000	—	pF
Output Capacitance	$V_{DS} = 50V$	C_{oss}	—	600	—	
Reverse Transfer Capacitance	$f = 1 \text{ MHz}$	C_{rss}	—	—	—	

CASE OUTLINE: Flat Pack (FP) - 12 Pin Package



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