Solid State Devices, Inc.
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Phone: (562) 404-4474 * Fax: (562) 404-1773
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SFS3027 - SFS3029 Series

0.5 AMP, 30 - 100 Volt FAST SWITCHING SILICON CONTROLLED RECTIFIER

Designer's Data Sheet

Part Number/Ordering Information [1/]

SFS302 ___ ___ ___

Screening [2/]
- ___ = Not Screened
- TX = TX Level
- TXV = TXV
- S = S Level

Package
- S.22 = SMD.22
- /18 = TO-18

Voltage/Family
- 7 = 30V
- 8 = 60V
- 9 = 100V

FEATURES:
- Passivated Planar Construction
- Low On-State Voltage and Fast Switching
- Hermetically Sealed Surface Mount Power Package
- Replacement for 2N3027 – 2N3029 Series - Contact Factory for Additional SCR Products

MAXIMUM RATINGS [3/]		Symbol	Value	Units
Peak Repetitive Reverse Voltage and DC Blocking Voltage	SFS3027 SFS3028 SFS3029	V_{DRM} V_{RRM}	30 60 100	**Volts**
Non-Repetitive Peak Reverse Blocking Voltage (t < 5.0 ms)	SFS3027 SFS3028 SFS3029	V_{RSM}	50 100 200	**Volts**
RMS On-State Current, (All Conduction Angles, T_C = 100°C)		$I_{T\ (RMS)}$	0.5	**Amps**
Peak Non-Repetitive Surge Current (One Cycle, 60 Hz)		I_{TSM}	8	**Amps**
Peak Gate Power		P_{GM}	0.1	**Watts**
Average Gate Current		$I_{G(ave)}$	0.025	**Amps**
Peak Gate Current		I_{GM}	0.25	**Amps**
Reverse Gate Current		I_{GR}	0.003	**Amps**
Reverse Gate Voltage		V_{GM}	5.0	**Volts**
Operating Junction Temperature Range		T_J	-65 to +150	**°C**
Storage Temperature Range		T_{stg}	-65 to +200	**°C**
Thermal Resistance, Junction to Case		$R_{\theta JC}$	15	**°C/W**

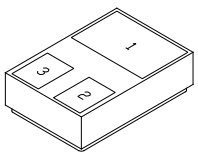
NOTES:

1/ For ordering information, price, operating curves, and availability- Contact factory.

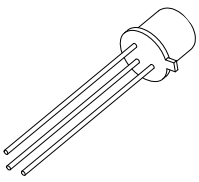
2/ Screening based on MIL-PRF-19500. Screening flows available on request.

3/ Unless otherwise specified, all electrical characteristics @25°C.

SMD.22



TO-18



NOTE: All specifications are subject to change without notification. SCD's for these devices should be reviewed by SSDI prior to release.	**DATA SHEET #: SCR010D**	**DOC**

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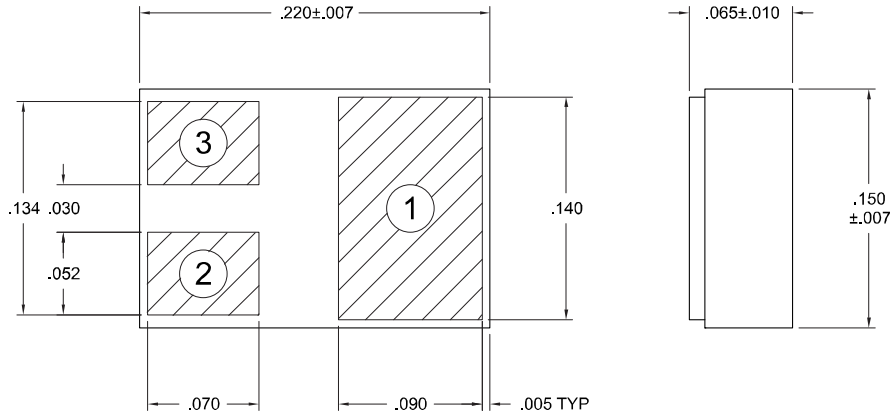
ELECTRICAL CHARACTERISTICS[3/]		Symbol	Min	Typical	Max	Unit
Peak Reverse Blocking Current Rated V_{RRM}, R_{GK} = 1000 Ω	T_C = 25°C T_C = 150°C	I_{RRM}	—	0.08 20	0.1 50	µA
Peak Forward Blocking Current Rated V_{DRM}, R_{GK} = 1000 Ω	T_C = 25°C T_C = 150°C	I_{DRM}	—	0.08 30	0.1 50	µA
Peak On-State Voltage I_F = 1.0 A pulse		V_{TM}	0.8	1.1	1.5	V
Gate Trigger Current V_D = 5 V_{DC}, R_L = 100 Ω, R_e = 10 kΩ	T_C = 25°C T_C = -65°C	I_{GT}	— —	25 50	200 1200	µA
Gate Trigger Voltage V_D = 5 V_{DC}, R_L = 100 Ω, R_e = 100 Ω	T_C = 25°C T_C = -65°C T_C = 150°C	V_{GT}	0.4 0.6 0.1	0.55 0.75 0.20	0.8 1.1 0.6	V
Holding Current V_D = 5 V_{DC}, R_{GK} = 1000 Ω	T_C = 25°C T_C = -65°C T_C = 150°C	I_H	0.3 0.5 0.05	1.0 1.5 0.38	5.0 10.0 1.0	mA
Off-State Voltage-Critical Rate of Rise		dv_c/dt	30	—	—	V/µs
Gate Trigger-on Pulse Width Per Fig. 1		$t_{pg(on)}$	—	0.25	0.40	µs
Gate Trigger-on Delay Time **Gate Trigger-on Rise Time** Per Fig. 1 with C1 = 0 and C2 = 0		t_d t_r	— —	0.10 0.75	— —	µs

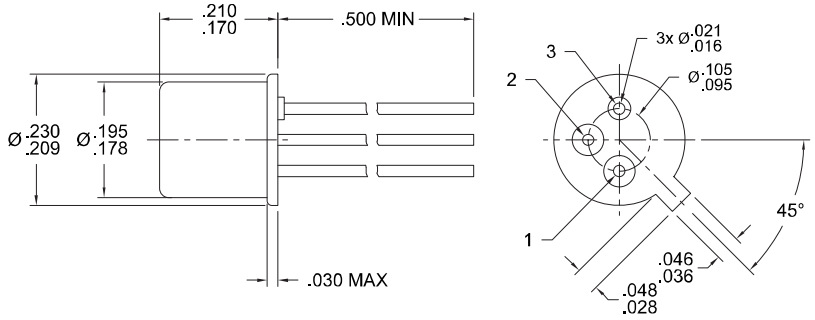
Case Outline: SMD.22

PAD 1: ANODE
PAD 2: CATHODE
PAD 3: GATE



Case Outline: TO-18

PIN 1: CATHODE
PIN 2: GATE
PIN 3: ANODE



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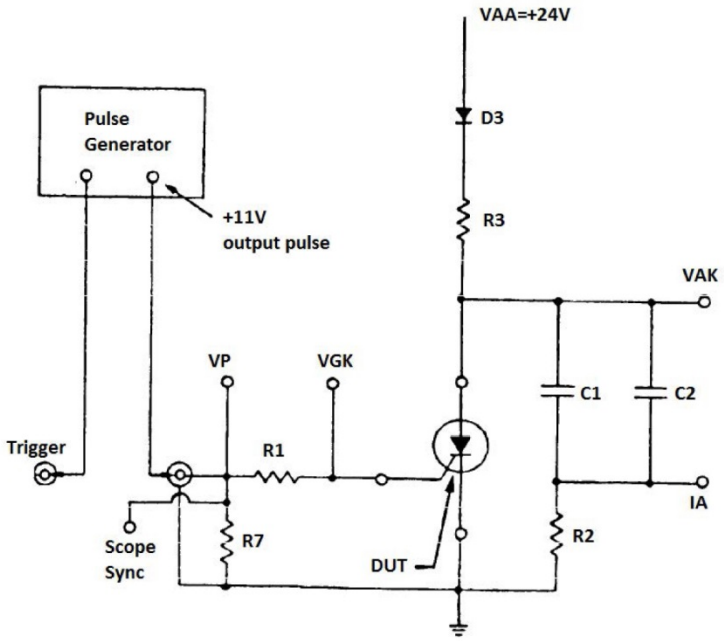

Fig. 1 Test Circuit for tpg(on), td and tr

Legends of circuit Element: R1=1k, R2=30 non-inductive, R3=500 2W, R7=56, C1=1uF, C2=0.1uF ceramic, D3=1N457A (optional)

tpg(on) Test Procedure:
1. Can use DC or pulsating AC 60Hz for VAA. If VAA is pulsating AC then D3 must be used, and trigger to Pulse Gen should be synchronized.
2. With specified VAA, IF and IGF initially established, connect a high frequency oscilloscope vertical input to the IA monitor point. The width of the gate current pulse is then set to a value that causes triggering to occur. The pulse width at this point is the gate trigger-on pulse width.
3. For addtional details, see Mil-S-19500/419(EL).

td and tr Test Procedure:
1. Remove C1 and C2, and set gate pulse width >2us.
2. Measure td from leading edge of gate pulse to 10% of VAK falling edge.
3. Measure tr from 10% to 90% of VAK falling edge.